Class-D Audio Amplifier with a 5-Band Equalizer

Final Project Report

May 15-24

Alan Stewart, Dana Conrad
Troy Bowers, Kyle Maginot
Jing Li, Xilu Wang
Advisor/Client: Prof. Ayman Fayed

4/29/2015

This page intentionally left blank.

Table of Contents

Team

Client/Advisor:

Ayman Fayed aafayed@iastate.edu

Team Info

Bowers, Troy Lynn, Communicator
tlbowers@iastate.edu
702-481-5777

Conrad, Dana Jay
dconrad@iastate.edu
319-830-3109

Li, Jing, Key Concept Holder
kobelk@iastate.edu
515-708-0218

Maginot, Kyle Paul
kyle0729@iastate.edu
630-532-9026

Stewart, Alan Autry, Leader
alans@iastate.edu
712-943-1525

Wang, Xilu, Webmaster
xiluw@iastate.edu
515-817-3852

List of Figures

List of Tables

Abbreviations

EQ- Equalizer
LPF- Low Pass Filter
HPF- High Pass Filter
BPF- Band Pass Filter
IC - Integrated Circuit
I/O- Input and Outputs
LED - Light Emitting Diode
MOSFET - Metal Oxide Semiconductor Field Effect Transistor

Op Amp- Operational Amplifier
PCB - Printed Circuit Board
SNR - Signal to Noise Ratio

Executive Summary

This project targets the implementation of a class-D audio amplifier system with a 5-band equalizer. An audio signal is to be sent through an equalizer system that can emphasize or de-emphasize certain bands and then be amplified via a switching amplifier to 200 Watts RMS.

System Design

Block Diagrams

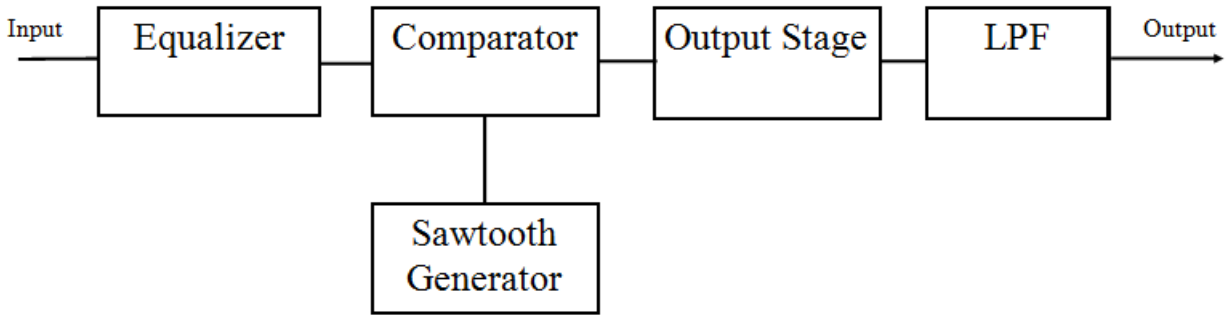


Figure 1. System Block Diagram

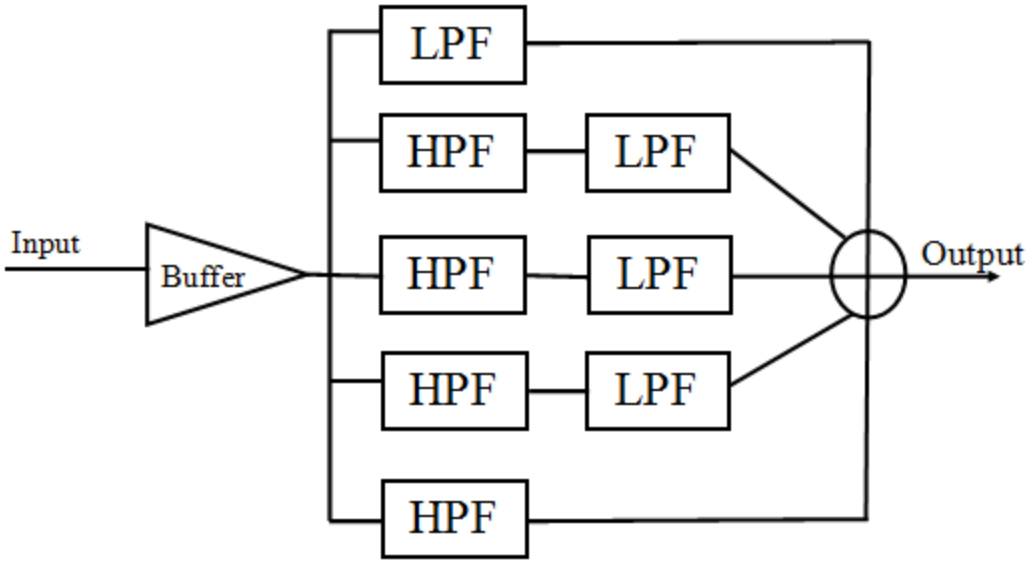


Figure 2. Equalizer Block Diagram

Requirements:

Functional

Class-D amplifier

A Class-D amplifier is a required component. The Class D amplifier will provide high-efficiency, high-power amplification of an audio signal. This signal will then be used to drive a speaker system.

Equalizer

The equalizer will consist of five frequency bands. It will provide an interface for the user to adjust the amplitude of one or more frequency ranges independently of the others.

Our Equalizer system was only defined to process five audio bands. Beyond that definition, it was left up to us what the frequency specifications should be. We chose to break up the 20 Hz - 20 kHz spectrum into the following:

Filter	High-Pass 3dB Frequency	Low-Pass 3dB Frequency
Low Pass Filter	---	80 Hz
Low Band-Pass Filter	90 Hz	325 Hz
Middle Band-Pass Filter	300 Hz	900 Hz
High Band-Pass Filter	900 Hz	3000 Hz
High Pass Filter	4000 Hz	---

Table 1 - Final Filter Range Definition

Non-functional

SNR

This provides a measure of fidelity. A larger SNR means the signal strength is greater than any background noise in the system. Our project shall provide an SNR of at least 96 dB.

Power System

The output of the system shall be capable of providing a 200 Watt audio signal to the speaker load. This will provide ample power to drive speakers to high volumes.

Power System Efficiency

The overall power efficiency of the amplifier shall exceed 85% when providing full power to the speaker load.

Operability

The system shall provide an interface for the user to change the scaling factors of any EQ band, and there shall be visual indicators that shows the current band level.

Detailed Design

Class-D Amplifier

A Class D amplifier uses transistor switches that oscillate between on and off at very high frequencies to recreate the input signal. This process is accomplished by using PWM. The amplifier translates an incoming audio signal into a high power version of the audio signal. This is accomplished through a three stage process.

In the first stage, the audio signal is compared to a 800 kHz sawtooth wave. The comparator creates a pulse-width modulated square wave signal that represents a translation of the original audio signal.

In stage two this PWM signal is passed to a switching MOSFET stage. This stage consists of two MOSFETs. One is connected to the positive rail whilst the other is connected to the negative. The gates on the MOSFETS are driven by the PWM translated audio signal. This amplifies the signal to levels necessary to power the speaker system.

The final stage uses a low pass filter designed to eliminate the switching frequency noise and filter the PWM signal back into a sinusoidal signal. This final signal is an approximation of the original audio signal but is capable of powering a high output speaker system.

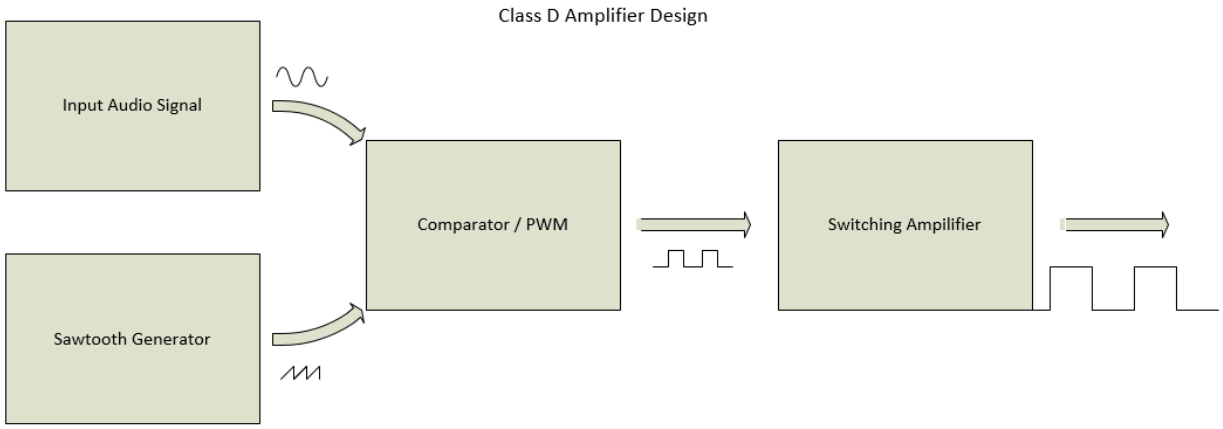


Figure 3. Class-D architecture Block Diagram

Sawtooth Generator

The sawtooth generator creates a waveform that can be used, in conjunction with the comparator, to produce a PWM signal. A sawtooth wave provides many advantages over a triangle wave, most importantly a decrease in duty cycle of the waveform and simplicity of design. By only including half of the triangle shape, we can save valuable power and increase efficiency. Since the generator will be running at 800 kHz, the square wave signal will be negligibly affected by the difference between the two waveforms.

Comparator

The Comparator uses the output of the sawtooth generator and compares it to the output of the Equalizer circuit. In this circuit, the EQ output has been replaced by a Sinusoid generator operating at 1 kHz in order to test the circuit's functionality.

Expected Output for this Circuit at 1 kHz (Sawtooth Trace Removed)

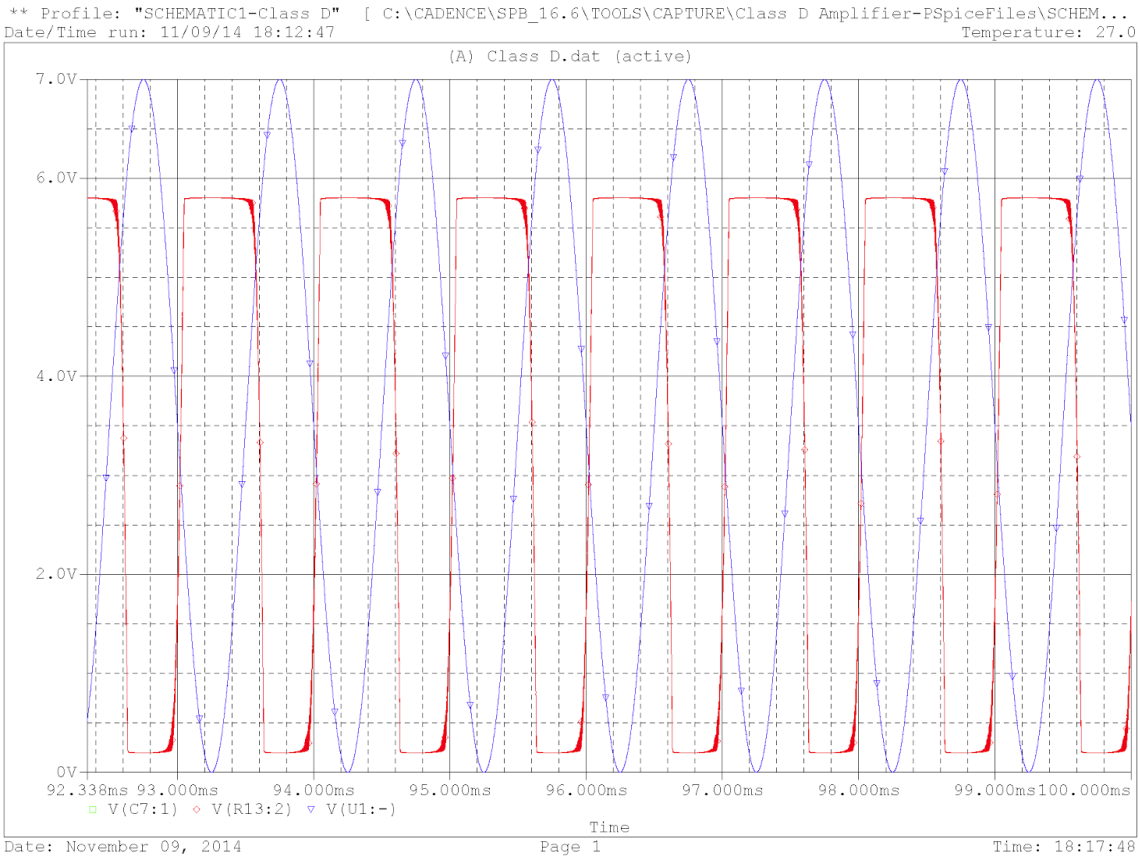


Figure 4. Simulated PWM output of a 1 kHz sine wave

Switching Stage

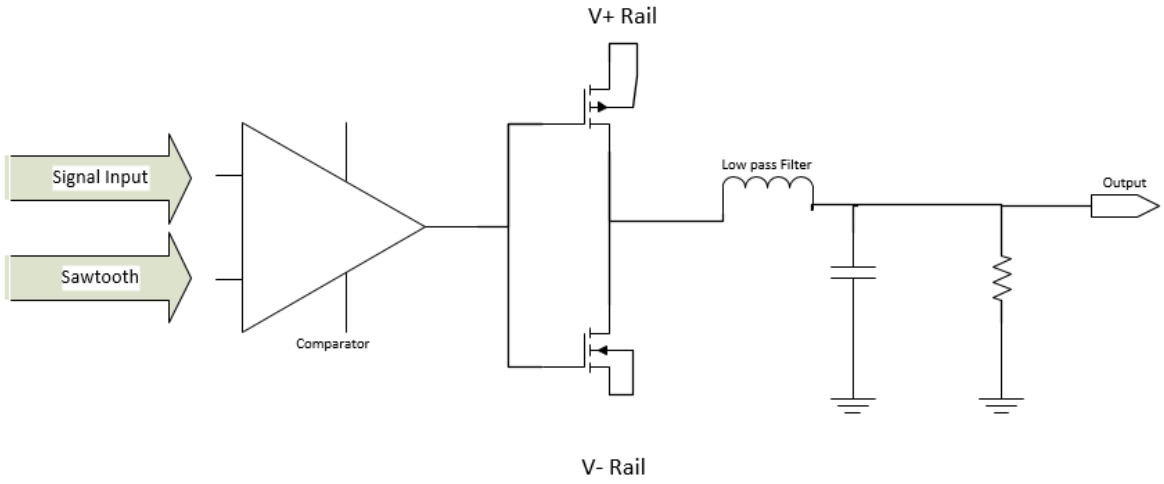


Figure 5. Simplified Switching Stage Schematic

The switching stage consists of a set of MOSFETS and a low pass filter. The PWM signal is used as the switching signal for the MOSFETs. By switching the MOSFETs we produce an amplified version of the PWM signal. A low pass filter converts this signal into an amplified version of the input.

Equalizer

Filter Design Process

Our filter design process is as shown in the *Analog Filter and Circuit Design Handbook*[1]. In this approach, we choose a normalized filter design with a 3dB frequency at 1 Hz. We then choose two values- a Frequency Scaling Factor (FSF) to convert the normalized filter into a denormalized filter at our desired frequency, and an impedance (Z) to transform the component values into realistic values. In a low-pass filter, this means our resistors are equal to Z, and each capacitor is

$$C_{n,denormalized} = C_n\left(\frac{1}{FSF*Z}\right)$$

Where C_n is a standard capacitance from a table out of the above book.

A low-pass filter can be transformed into a high-pass filter by swapping the locations of the capacitors and resistors. In this case, the capacitances are

$$C = \frac{1}{FSF * Z}$$

And the resistances are

$$R_{n,denormalized} = \frac{1}{C_n} * Z\,.$$

Because our band-pass filters are wider than a factor of (approximately) 2, they are a simple cascading of high- and low-pass filters, designed as described above.

Realized Filters

During the process of simulating the system as a whole, we ran into variation in the output level due to overlap in the bands. Even with fourth order filters, the attenuation roll-off is slow enough that one band may interfere with another two or even three bands over. To reduce these effects, we adjusted our 3dB frequencies as shown in the following tables.

[1] *Analog Filter and Circuit Design Handbook*, Williams, Arthur B., McGraw Hill. New York, 2014.

Initial Bands

Filter	High-Pass 3dB Frequency	Low-Pass 3dB Frequency
Low Pass Filter	---	180 Hz
Low Band-Pass Filter	150 Hz	325 Hz
Middle Band-Pass Filter	300 Hz	1000 Hz
High Band-Pass Filter	900 Hz	3000 Hz
High Pass Filter	3000 Hz	---

Table 2 - Initial Filter Range Definition

Current Bands

Filter	High-Pass 3dB Frequency	Low-Pass 3dB Frequency
Low Pass Filter	---	80 Hz
Low Band-Pass Filter	90 Hz	325 Hz
Middle Band-Pass Filter	300 Hz	900 Hz
High Band-Pass Filter	900 Hz	3000 Hz
High Pass Filter	4000 Hz	---

Table 1 - Final Filter Range Definition

Filter Schematics

We chose fourth order active filters which require two operational amplifiers, ideally four resistors, and four capacitors per high/low-pass filter. The number of components therefore doubles when a band-pass filter is required. The schematics are available in Appendix V.

Simulations

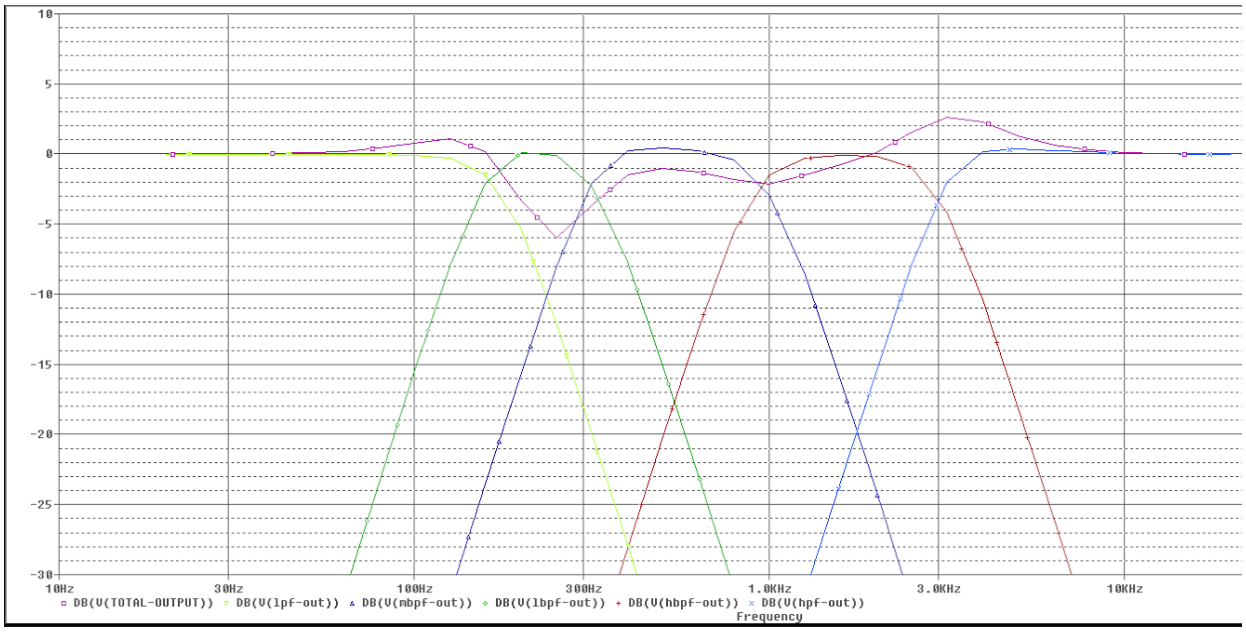


Figure 6. Initial Overall Filter Simulation

This is the pre-realized filter simulation. At this stage we discovered very large variations in gain - approximately 9 dB - over the spectrum. The output is on average lower than 0dB.

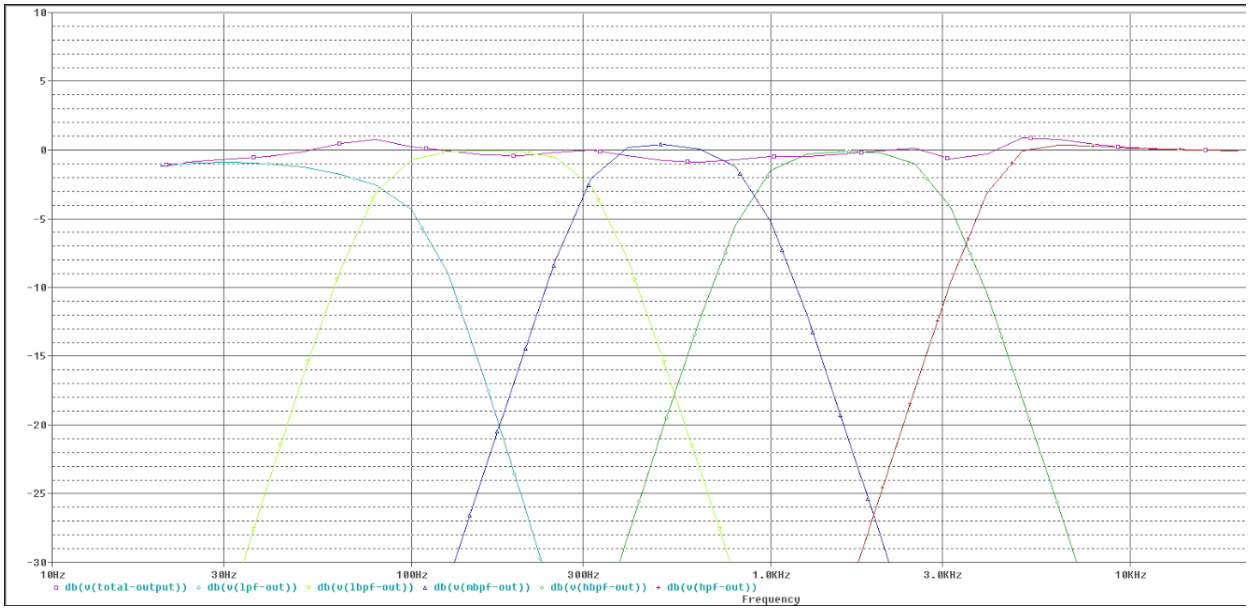


Figure 7. Final Overall Filter Simulation

Here is the new simulation after the adjustments in 3 dB frequencies. We see that the output is much flatter - within 1 dB of 0 dB across the spectrum. The level also changes less rapidly than in the original design.

Finally, we have the phase plot from simulation. As all our filters are Butterworth filters, the phase shift at the extreme ends of the spectrum is always a multiple of 180 degrees.

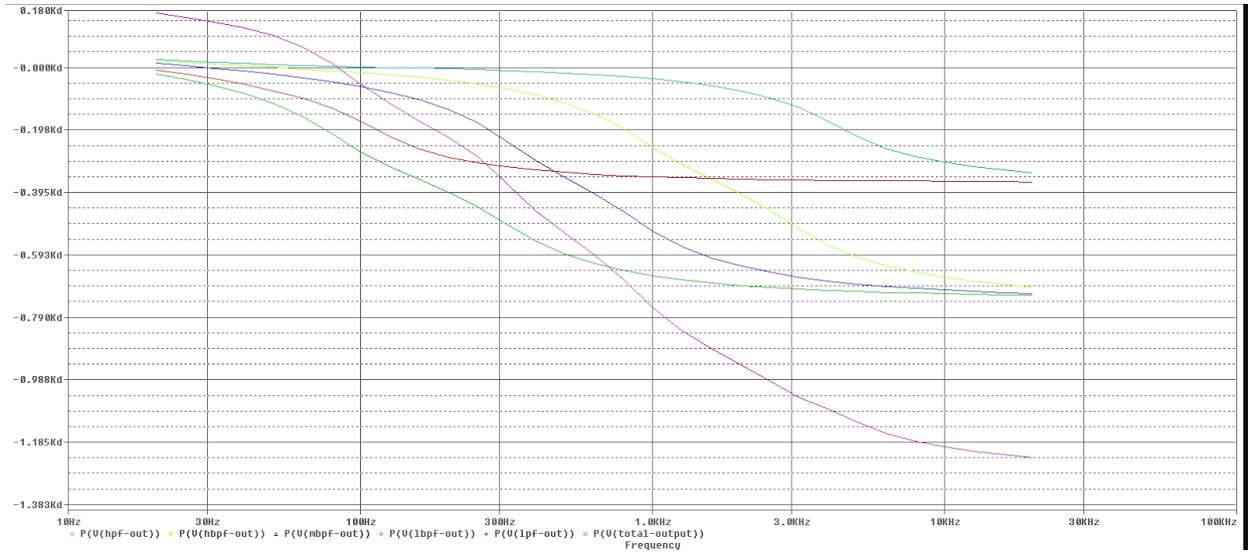


Figure 8. Filter Phase Response

Mixer Design

For the mixer, we use a summing amplifier with potentiometers to adjust the gain of individual bands. This is given by, in the case of the HPF,

$$\frac{R47}{R42 + R41}$$

where R41 is adjustable between 0 and 500 kΩ. Thus we are able to vary the gain between 0.25 and unity.

Mixer Schematic

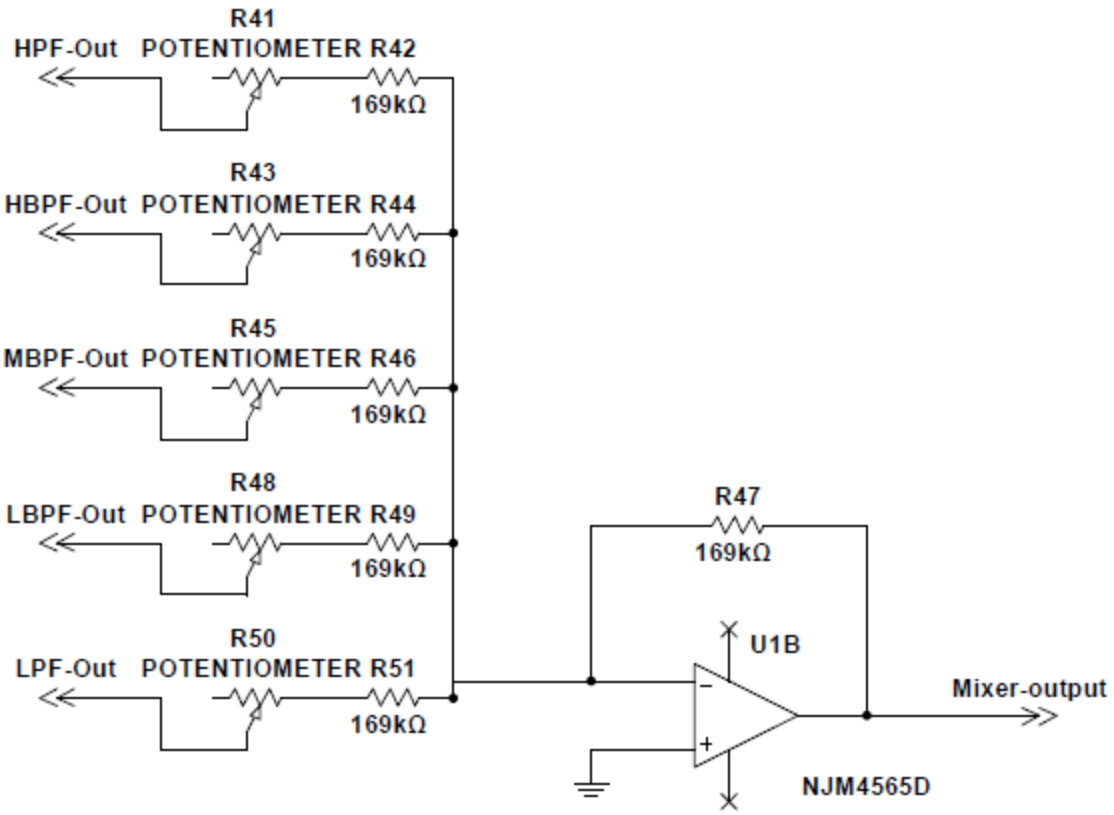


Figure 9. Mixer Schematic

Input Buffer

Our input buffer is a simple non-inverting op-amp stage with unity gain and a high-pass filter. This is to decouple our circuit from the input device for biasing purposes.

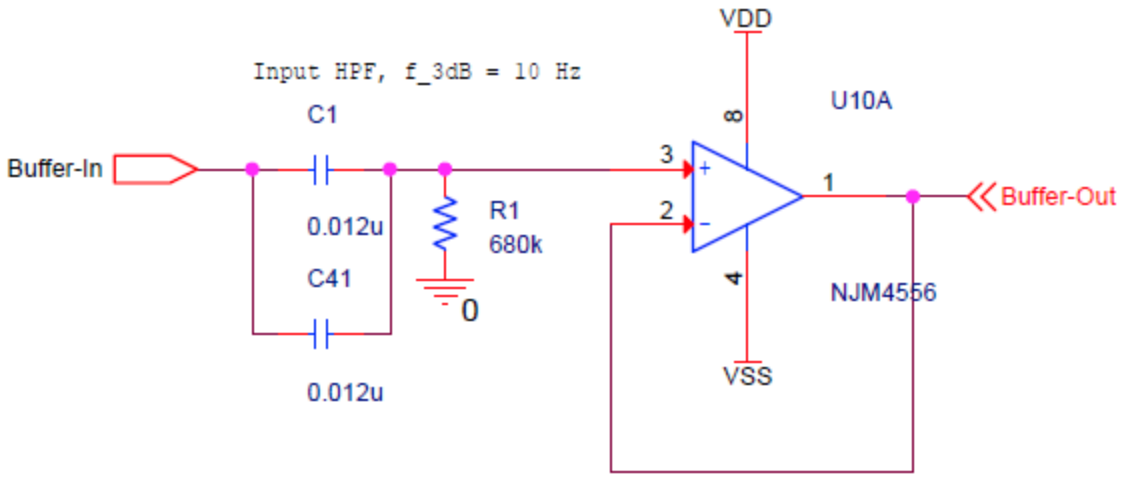


Figure 10. Input Buffer Schematic

User Interface

Our user interface consists of 5 ten-segment LEDs, as seen in Fig. 11, to give visual feedback of where the EQ controls are set. The LEDs are driven by an Arduino Mega, which reads a voltage between 0 and 5V from the B circuits on our dual-gang potentiometers. This voltage is then quantized into levels from 0 to 9, and then the appropriate LED is turned on in each bar graph. Our code for this system is available in Appendix IV.

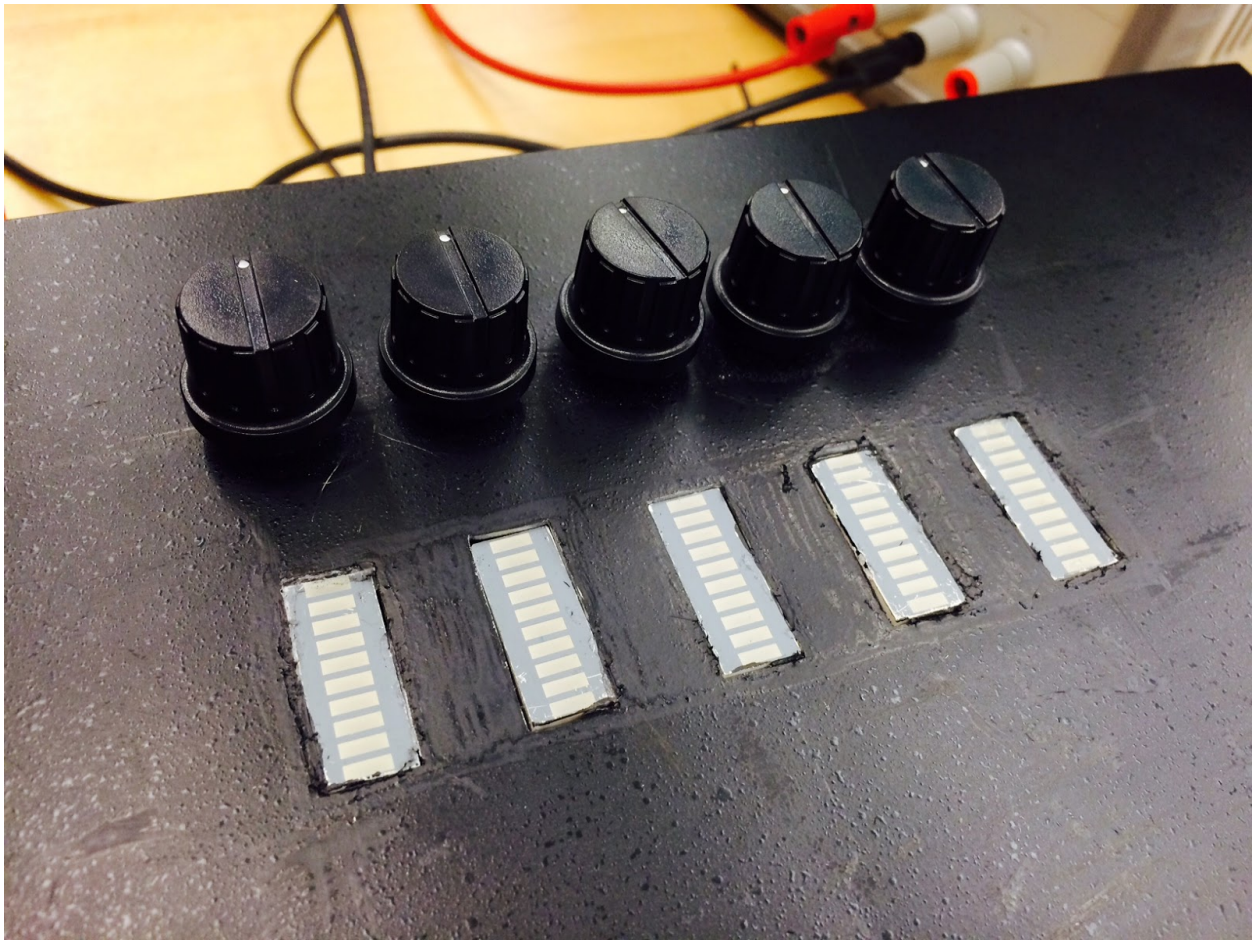


Figure 11. LED user interface

Signal Bypassing Switch

With the Signal Bypassing Switch, our user can choose to let the signal engage or bypass the equalizer. When it's on, our user can listen to the music under effect. When it's off, our user can listen to the original music without any effect. As a result, our user can easily distinguish the effects that an EQ can present to an audio signal.

PCB Design

Amplifier

The amplifier's central focus point is the IRS2092 IC.This IC allowed us to control for shoot through current and sawtooth non-linearity. From here we designed the components needed to achieve our intended power delivery and efficiency goals.

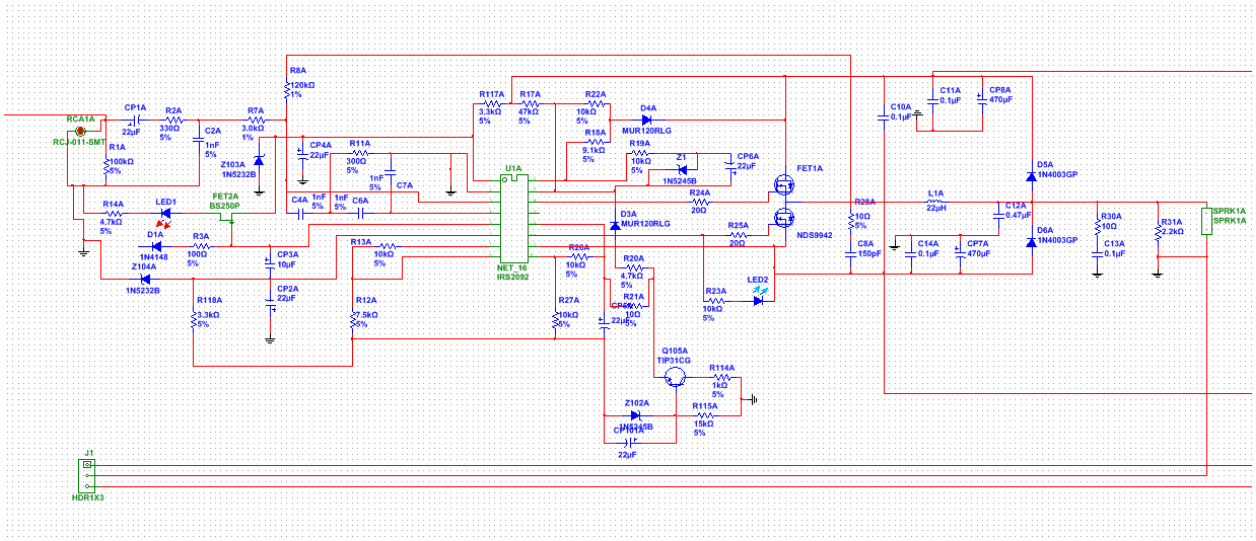


Figure 12. One-half of the Amplifier circuit

The PCB design began using Multisim software to build the circuit based around the gate driver IC. The circuit above shows the first half of the full-bridged design used to meet our power requirements. Once this circuit was completed in Multisim, it was passed to its affiliated program, Ultiboard, to begin the PCB construction.

Using Ultiboard, we were able to place the components selected during the Multisim design process on the board.Ultiboard allowed us to select board parameters and size dimensions. Unfortunately the dimensions reverted to 4.5" x 6" during design iterations, and greatly reduced the overall footprint available to us. We originally planned to have a 5" x 7" PCB for this component.

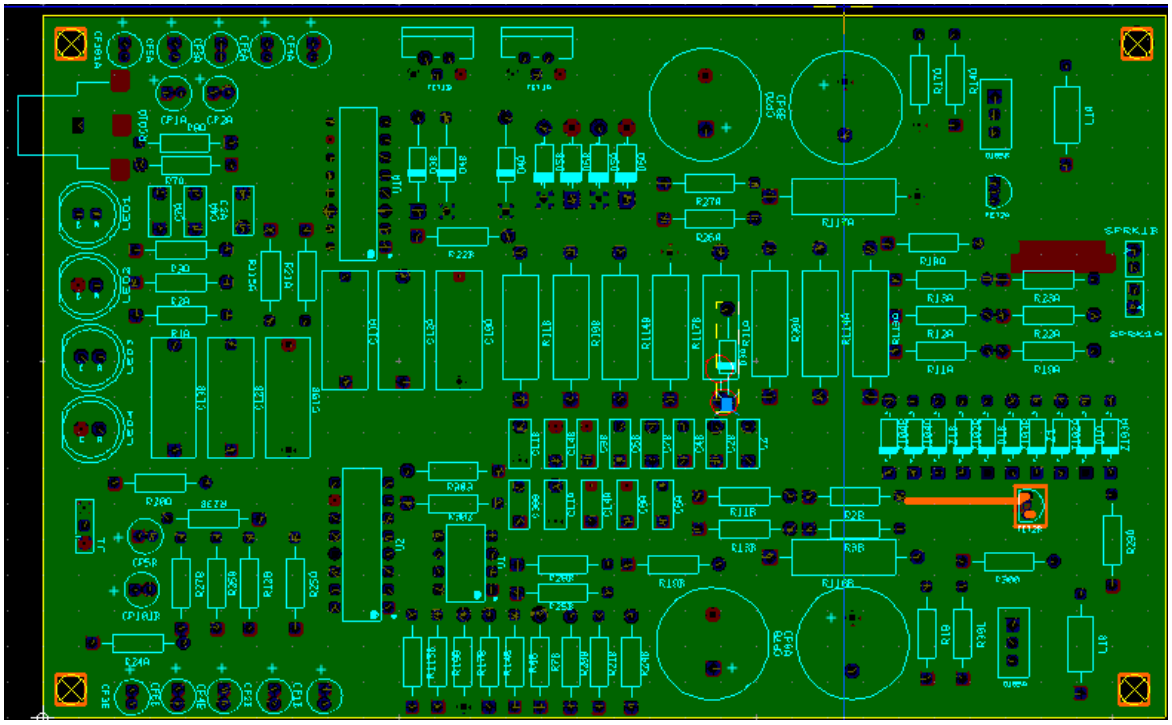


Figure 13. The amplifier PCB diagram

The parts were ordered through Mouser and Digikey. All of the components were hand soldered in place. The process took a few hours and required extreme attention to detail. We needed to ensure proper placement and quality connection. The major concerns were improper orientation and damaging the traces while soldering. We tackled the problem of component placing by having a two person, two step verification process. This required one person to handle the soldering of the components while the other used a print off of both the circuit diagram and the bill of materials to verify each part. As a part was removed from the packaging and verified against the circuit diagram it was then handed to the board solder attendant along with the PCB reference number. This process helped to minimize chances of improper component placement. Our second concern was to reduce heat load on the board. To accomplish this we avoided soldering adjacent components onto the board. By working varying areas of the board it was allowed to cool before being worked again. This helped to prevent thermal board fatigue and reduce the potential of damaging traces.

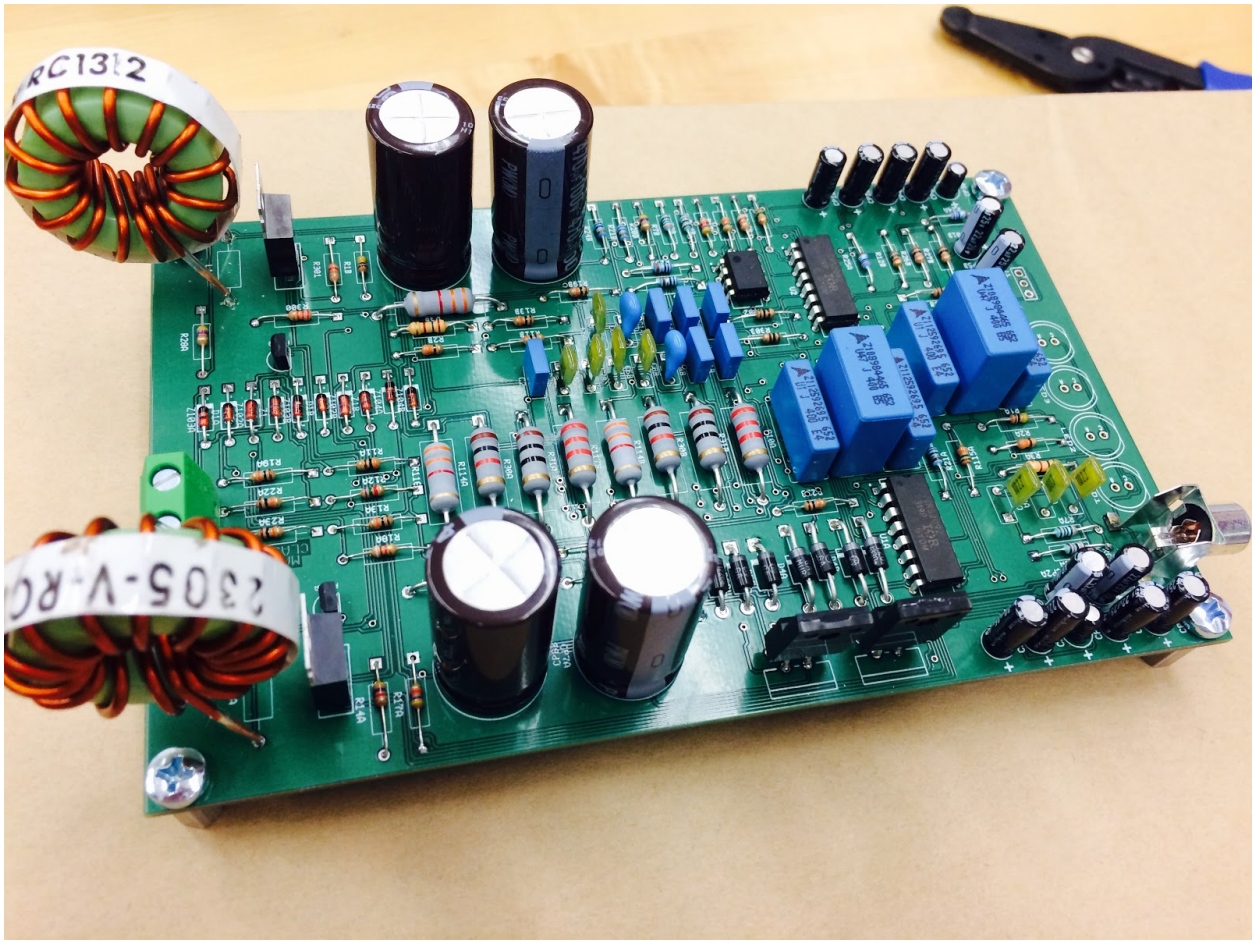


Figure 14. Populated PCB

Equalizer

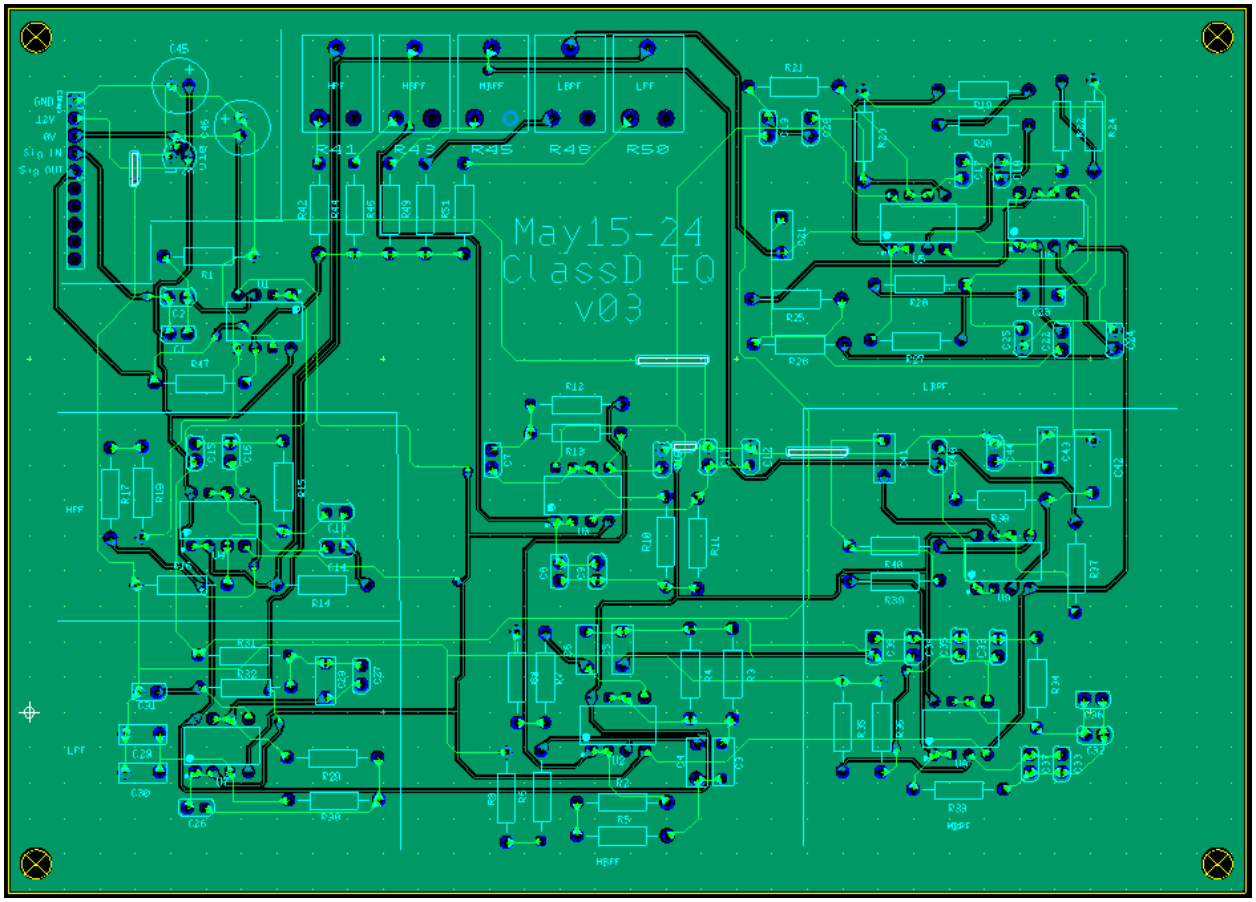


Figure 15. EQ PCB Design

This design is a double-sided PCB with a ground plane on the back of the board. We built each section independently so that we could take advantage of the autorouter functionality and still have some amount of routing optimization. After producing a part layout that we liked, we ran the autorouter. We found that the autorouter produced results that were only so good, and we adjusted many traces to be to our liking. We partitioned the board into sections so that it would be easy to diagnose if we ran into problems.

We designed this PCB entirely around through-hole parts for ease of construction. It was possible that we would have had to build several revisions, and through-hole technology is very quick to populate by hand. For a production version, we would redesign this for surface mount parts in order to bring the part density up significantly and reduce the size of the board.

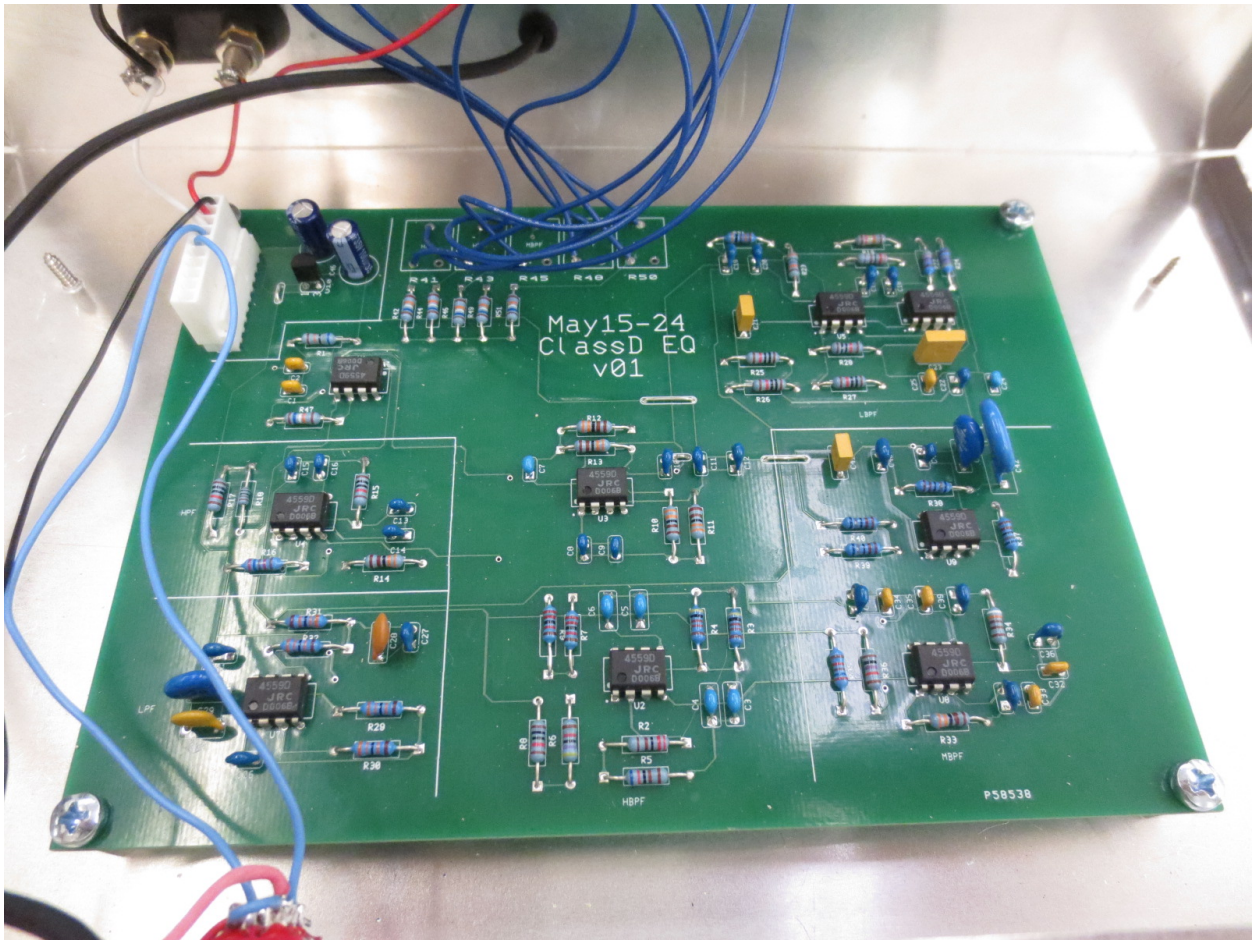


Figure 16. Completed EQ PCB

Figure 16 is our completed EQ PCB. The board is actually the third version revision, but due to an oversight we left the original version number.

Test Methods

SNR

We measure Signal to Noise Ratio by inputting a 1 kHz, 1 V_{RMS} sinusoid. We then measure the output sine wave amplitude (A) and the amplitude of the noise (N) on the output. Then we use the equation

$$SNR = 20\ log(\frac{A}{N}).$$

This value should be greater than 96 dB.

Power Efficiency

We measure the power efficiency by

$$Efficiency = \frac{Pout}{Pin + Peq} * 100$$

Where P_{OUT} is the measured power output, P_{IN} is the measured power input from the power supplies, and P_{EQ} is the power drawn by the Equalizer. We take this measurement at full power output, and do not count power dissipated by the power supplies.

This value should be greater than 85%.

Test Results

Amplifier Failure Analysis

Upon completion of the amplifier board, we began the testing process to determine the total power output as well as determine the total efficiency of the unit. Once plugged into the power supplies and turned on, there was a short in the PCB and momentary flash along one of the traces. The trace path where the burn occurred is highlighted below.

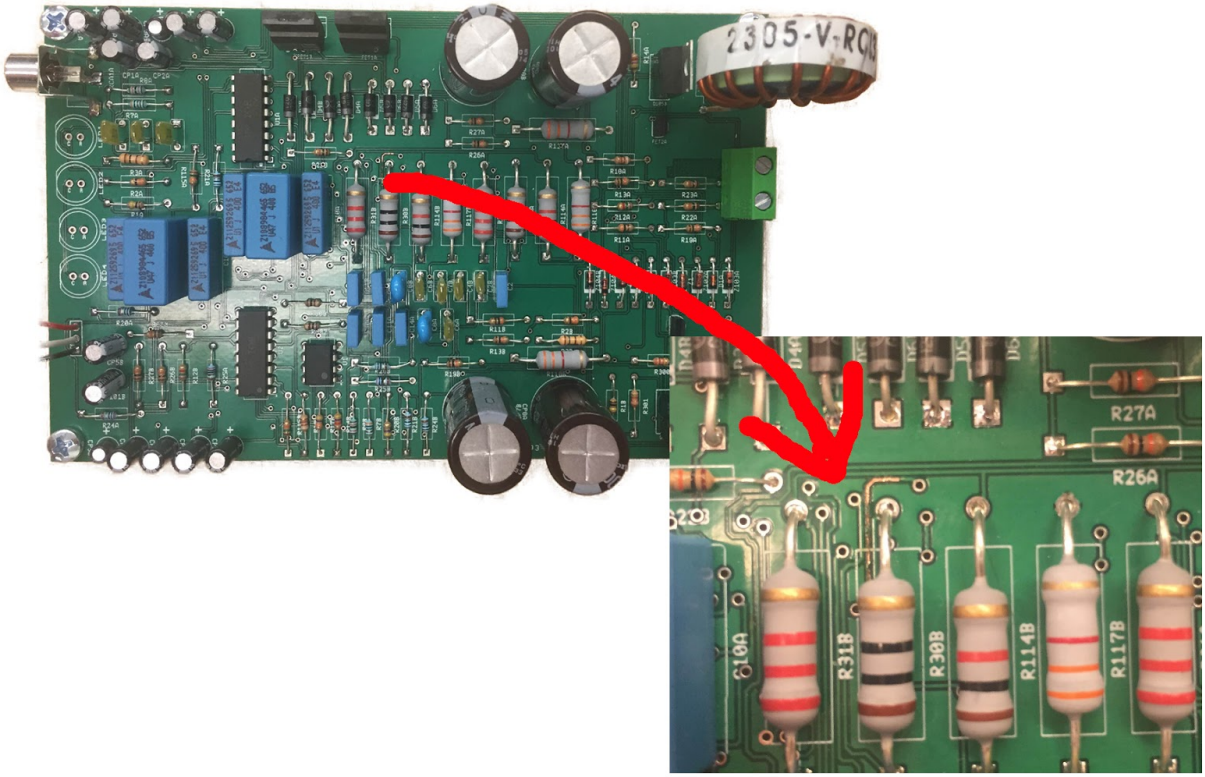


Figure 17. Amplifier Board Damage

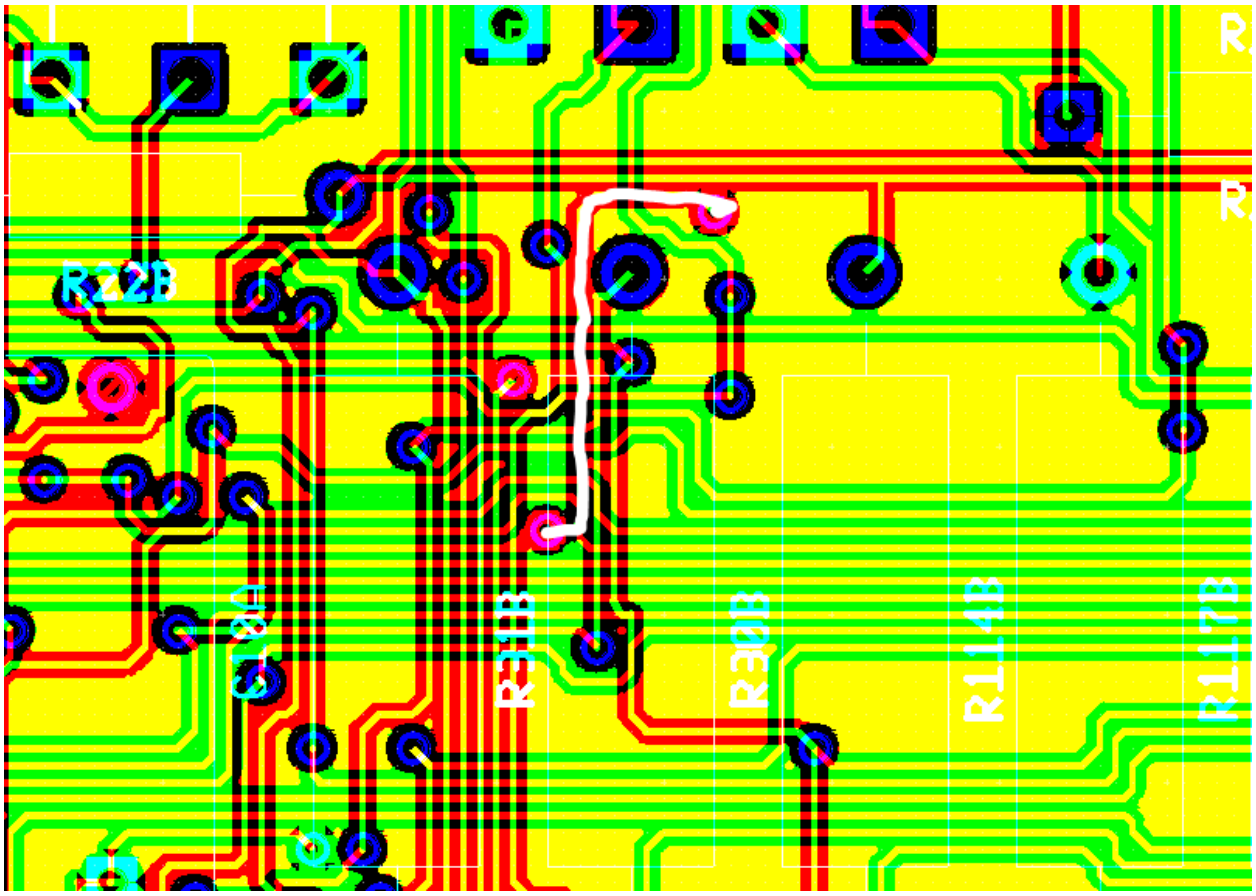


Figure 18. Amplifier PCB Problem Area

After seeing this flash, the unit was disconnected from power and fault analysis began. The white line drawn in the above circuit shows where the burn took place. This trace connects two portions of the +48V power plane. Due to the inrush current required to charge the capacitors at a location beyond this point, the trace overheated and failed due to insufficient conductor width. In future revisions of the amplifier board, the minimum trace width needs to be able to accommodate as much as a 5 Ampere current load. This number comes from the maximum output of the MOSFET to be delivered to the load and any transient charging current.

Power Efficiency

Due to the fault of the amplifier board, we can only calculate a theoretical power efficiency of the amplifier system. A class D amplifier's design allows for a 100 percent theoretical efficiency, but we know what this is not the case. The reason that a class D amplifier can not be perfectly efficient is due to the rise and fall time of the components as they reach their 'On' and 'Off' states. This period where the gate drivers and MOSFETs are experiencing voltage output without power being delivered to the load is the primary source of waste power.

The datasheet for the MOSFETs give a rise and fall time of 6.6 nS and 3.1 nS respectively. Coupling this with the rise and fall times associated with the gate driver (20 nS and 15 nS) and the built in dead time delay (25 nS) we have a total of 69.7 nS of wasted power delivery per cycle. The 800 kHz sawtooth waveform generated by the gate driver produces a period of 1.25 uS. Using this number as our base, we can derive a 5.576% power loss during transient periods of the amplifier switching. Being well aware of other possible losses in the system, we can confidently double this loss to include an acceptable range of other contributing factors. Even with a total of 11.152% loss of power in amplifier performance, we see the inverse reaching above our original required target of 85% at a successful 88.848% efficiency.

Signal to Noise Ratio

Unfortunately, without the power gain from an amplifier we are unable to measure the SNR of our Equalizer system. Our plan was to measure the SNR at the output with a 1 kHz, 1 V_{RMS} input. However, with our EQ system having a maximum possible output of 12 V_{PP} versus an amplifier output of 96 V_{PP}, this would require a noise amplitude of 190 μV_{PP}. We ran into two problems when we attempted to measure this. The first is that the signal generator available to us is not capable of producing that accurate of a signal. Our signal generator is only capable of producing a signal accurate to within 1% of the desired output, and we need accuracy on the order of 0.01%. The second problem we ran into is even if we were able to design a test to get around the poor accuracy of our signal generator, we are unable to find how accurate the oscilloscope we have available to us is at the 0.1 mV_{PP} level.

Final Product

Even with the failure of our amplifier board, we were able to complete half of the project. The Equalizer has been tested and verified as working properly. In order to have a demonstration of how well our equalizer works, we purchased a commercial amplifier of similar specifications to what we sought to achieve. Figure 19 shows our finished equalizer in its enclosure.

Figure 19. Finished equalizer

Bill of Materials

Amplifier

Qty.	Value	Description	Part Number	Unit cost	Extended Cost
8	1nF, 50V	CAP 1nF 50V POLYESTER 5%	493-3443-ND	$0.32	$2.56
2	150 pF, 250V	CERAMIC CAP 150PF 250 VAC CERAMIC 10 %	490-9429-ND	$0.30	$0.60
2	Open	CERAMIC CAP 150PF 250 VAC CERAMIC 10 %	594-S151K33Y5PR63 K7R	$0.10	$0.20

4	0.1uF, 400V	CAP .10UF 400V METAL POLYPROPYLANE	495-1311-ND	$0.76	$3.04
2	0.47uF, 400V	CAP .47UF 400V METAL POLYPROPYLANE	495-1315-ND	$1.00	$2.00
4	0.1uF 100V	CAP .10UF 100V	495-1147-ND	$0.32	$1.28
2	0.1uF 100V	CAP .10UF 100V	495-1147-ND	$0.32	$0.64
1	ED365/3	TERMINAL BLOCK 7.50MM 3POS PCB	ED2355-ND	$1.44	$1.44
12	22uF	CAP 22UF 25V ELECT VR RADIAL	493-1058-ND	$0.23	$2.76
2	10uF, 16V	CAP ELECT 10UF 16V KS RADIAL	P966-ND	$0.26	$0.52
4	470uF/100V	CAP 470UF 100V ELECT PW RADIAL	493-1985-ND	$1.89	$7.56
1	330uF, 10V	CAP 330UF 10V ALUM LYTIC RADIAL	P5125-ND	$0.25	$0.25
2	1N4148T-73	DIODE SWITCH 100V 150MA DO-35	1N4148-TPMSCT-ND	$0.10	$0.20
4	MUR120RLG	DIODE ULTRA FAST 1A 200V AXIAL DO-41	MUR120RLGOSCT-ND	$0.56	$2.24
4	1N4003	DIODE GEN PURPOSE 200V 1A DO41	1N4003FSCT-ND	$0.18	$0.72
2	BS250P	MOSFET P-CH 45V 230MA TO-92	BS250P-ND	$0.88	$1.76
2	22uH, 16.4A	Class D Inductor, 22UH	M8881-ND	$3.19	$6.38
2	Blue LED	LED 3MM DUAL	160-1602-ND	$0.94	$1.88
2	Red LED	LED 3MM HI-EFF RED	160-1140-ND	$0.33	$0.66
2	TIP31C	TRANS NPN EPITAX 100V 3A TO-220	TIP31CFS-ND	$0.54	$1.08

4	100k	RES 100K OHM	S100KQCT-ND	$0.10	$0.40
2	330	AXIAL RES 330 OHM	S330QCT-ND	$0.10	$0.20
2	100	AXIAL RES 100 OHM	S100QCT-ND	$0.10	$0.20
2	3k 1%	AXIAL RES METAL FILM 3.00K OHM 1/4W	S3KCACT-ND	$0.14	$0.28
2	120k 1%	AXIAL RES METAL FILM 120K OHM 1/4W	S120KCACT-ND	$0.14	$0.28
2	300	AXIAL RES 300 OHM CARBON FILM 1/4W 5%	S300QCT-ND	$0.10	$0.20
2	7.5k	AXIAL RES 7.5K OHM CARBON FILM 1/4W 5%	S7.5KQCT-ND	$0.10	$0.20
12	10k	AXIAL RES 10k OHM CARBON FILM 1/4W 5%	S10KQCT-ND	$0.10	$1.20
4	4.7k	AXIAL RES 4.7K OHM CARBON FILM 1/4W 5%	S4.7KQCT-ND	$0.10	$0.40
2	47k	AXIAL RES 47K OHM CARBON FILM 1/4W 5%	S47KQCT-ND	$0.10	$0.20
2	9.1k	AXIAL RES 9.1K OHM CARBON FILM 1/4W 5%	S9.1KQCT-ND	$0.10	$0.20
2	4.7	AXIAL RES 4.7 OHM CARBON FILM 1/4W 5%	S4.7QCT-ND	$0.10	$0.20
6	10	AXIAL RES METAL FILM 10.0 OHM 1/2W 1%	PPC10.0XCT-ND	$0.31	$1.86
4	20R	AXIAL RES METAL FILM 20.0 OHM 1/2W 1%	PPC20.0XCT-ND	$0.31	$1.24
2	10 1W	AXIAL RES 10 OHM 1W 5% METAL	10W-1-ND	$0.25	$0.50

		OXIDE			
2	2.2k 1W	AXIAL RES 2.2k OHM 1W 5% METAL OXIDE	2.2KW-1-ND	$0.25	$0.50
2	1k 1W	AXIAL RES 1.0K OHM 1W 5% METAL OXIDE	1.0KW-1-ND	$0.25	$0.50
2	15k	AXIAL RES 15K OHM 1W 5% METAL OXIDE	S15KQCT-ND	$0.10	$0.20
4	3.3k 1W	AXIAL RES 3.3K OHM 1W 5% METAL OXIDE	3.3KW-1-ND	$0.25	$1.00
2	22k	AXIAL RES 22K OHM CARBON FILM 1/4W 5%	S22KQCT-ND	$0.10	$0.20
2	100	AXIAL RES 100 OHM CARBON FILM 1/4W 5%	S100QCT-ND	$0.10	$0.20
1	RCJ-013	CONN RCA JACK	CP-1402-ND	$0.96	$0.96
1	RCJ-012	CONN RCA JACK	CP-1401-ND(Red)	$0.96	$0.96
1	EG2209A	SWITCH SLIDE DPDT	EG1908-ND	$0.95	$0.95
2	ED365/2	TERMINAL BLOCK	ED2354-ND	$1.03	$2.06
1	TL071CP	IC LN JFET-IN GP OP AMP 8-DIP	296-7186-5-ND	$0.62	$0.62
4	15V	Diode Zener 500 MW 15V DO35	1N5245B-TPCT-ND	$0.14	$0.56
4	5.6V	Diode Zener 500 MW 5.6 DO35	1N5232BVSCT-ND	$0.19	$0.76
2		11.9" x 7.5" x 2.9" Low-Profile Aluminum Instrument Enclosure		$17.95	$35.90
4		MOSFET 2N-CH 150V 8.7A TO-220FP	IRFI4019H-117P-ND	$3.75	$15.00
2		Mean Well Power		$71.61	$143.22

		supply			
				Total	$248.92

Table 3. Amplifier Bill of Materials

Equalizer

Qty.	Value	Reference	Part #	Unit Cost	Extended Cost
2	0.012u	C1, C2	81-RCE5C1H123J1K1H3B	$0.67	$1.34
4	8200p	C3, C4, C5, C6	81-RDE5C1H822J1S1H3A	$0.43	$1.72
2	0.018u	C7, C24	81-RCE5C1H183J1A2H3B	$0.67	$1.34
3	0.022u	C8, C9, C43	810-FK28X7R1H223K	$0.29	$0.87
2	0.015u	C10,C26	810-FK18X7R2A153K	$0.34	$0.68
1	560p	C11	810-FK18C0G1H561J	$0.35	$0.35
11	5600p	C12, C17, C18, C19, C20, C27, C31, C36, C37, C38, C39, C13, C14, C15, C16	810-FK14C0G1H562J	$0.40	$4.40
4	3900p	C13,C14,C15,C16	810-FK28C0G1H392J	$0.33	$1.32
1	0.028u	C21	581-CK05BX273K	$0.34	$0.34
1	0.1u	C22	810-FK28X7R1H104K	$0.30	$0.30
1	0.056u	C23	581-CK06BX563K	$0.47	$0.47
5	0.047u	C25,C32,C33,C34,C35	810-FK26X7R2E473K	$0.45	$2.25
1	1000p	C28	594-D102K29X5FL63L6R	$0.25	$0.25
2	2200p	C28, C44	75-WYO222MCMBF0KR	$0.32	$0.64
1	100p	C30	594-S101K29S3NN63L6R	$0.46	$0.46
1	0.068u	C40	810-FK26X7R2A683K	$0.44	$0.44
1	0.027u	C41	581-CK05BX273K	$0.34	$0.34
1	10000p	C42	810-CS14-F2GA103MYGK	$0.81	$0.81
2	100u	C45,C46	667-ECA-1VM101	$0.26	$0.52

1	680k	R1	660-MF1/4DC6803F	$0.12	$0.12
2	2.2k	R2, R20	660-MF1/4CCT52R2201F	$0.19	$0.38
2	40.2k	R3, R4	660-MF1/4DCT52R4022F	$0.12	$0.24
1	6.2k	R5	660-MF1/4DC6201F	$0.12	$0.12
1	47k	R6	660-MF1/4DC4702F	$0.12	$0.12
2	22k	R7, R9	660-MF1/4DCT52R2202F	$0.12	$0.24
7	10k	R8,R15,R17,R25,R26,R27,R28	660-MF1/4DC1002F	$0.12	$0.84
6	3.3k	R10,R11,R12,R13,R14,R33	660-MF1/4DC3301F	$0.12	$0.72
2	26.1k	R16,R35	660-MF1/4DCT52R2612F	$0.12	$0.24
1	1k	R18	660-MS1/4DCT52R1001	$0.10	$0.10
1	124k	R19	660-MF1/4D52R1243F	$0.12	$0.12
1	301k	R21	660-MF1/4D52R3013F	$0.12	$0.12
2	432k	R22,R24	660-MF1/4DCT52R4323F	$0.12	$0.24
1	357k	R23	660-MF1/4DC3573F	$0.12	$0.12
4	330k	R29,R30,R31,R32	660-MF1/4DCT52R3303F	$0.12	$0.48
1	9.31k	R34	660-MF1/4DC9311F	$0.12	$0.12
1	10.7k	R36	660-MF1/4DCT52A1072F	$0.12	$0.12
4	6.8k	R37,R38,R39,R40	660-MF1/4DCT52R6801F	$0.12	$0.48
5	500k pot, dual-gang	R41,R43,R45,R48,R50	PDB182-K420K-504B-ND	$1.91	$9.55
6	169k	R42,R44,R46,R47,R49,R51	660-MF1/4DC1693F	$0.12	$0.72
9	NJM4559	U1,U2,U3,U4,U5,U6,U7,U8,U9	513-NJM4559D	$0.71	$6.39
1	TLE2426	U10	595TLE2426ILP	$2.21	$2.21
1	22-23-2101 10 pin header	CONN1	538-22-23-2101	$0.59	$0.59

1	22-01-3107 10 pin housing	Not On Board	538-22-01-3107	$0.48	$0.48
5	08-50-0114	Crimp terminals	538-08-50-0114	$0.13	$0.65
1	STPX-3501-3C	TRS Stereo Jack	806-STPX-3501-3C	$1.27	$1.27
				Total	$45.62

Table 4. Equalizer Bill of Materials

LED User Interface

Qty	Desciption	Part number	Unit Cost	Extended Cost
50	User interface resistors	660-MS1/4DCT52R1001	$0.10	$5.00
1	Arduino, used as microconroller	Arduino Mega 2560 R3	$45.95	$45.95
5	10 Segment LED	604-DC10GWA	1.99	$10.00
			Total	$60.95

Table 5. LED User Interface Bill of Materials

Miscellaneous

Qty	Description	Part number	Unit Cost	Extended Cost
1	input jack, 3.5mm	806-STPX-3501-3C	$1.27	$1.27
1	EQ power input binding post BLACK	530-111-0103-1	$3.28	$3.28
1	EQ power input binding post RED	530-111-0102-1	$3.12	$3.12
1	amp out 1/4"	SC1085-ND	$3.05	$3.05

	jack			
5	EQ control dual-gang pots, 500k	PDB182-K420K-504B-ND	$1.91	$9.55
6	Knobs	450-2061	$0.60	$3.60
1	EQ bypass switch, DPDT	691-2M1-DP1-T1B1M1QE	$3.17	$3.17
1	machine screws, m4, 5mm, 100 pack	92005A212	$4.58	$4.58
8	F/F standoffs, m4, 12mm	95947A221	$0.63	$5.04
2	Grommet	RP450-ND	$1.77	$3.54
			Total	$40.20

Table 6. Miscellaneous Bill of Materials

Total Cost of one unit: $395.69

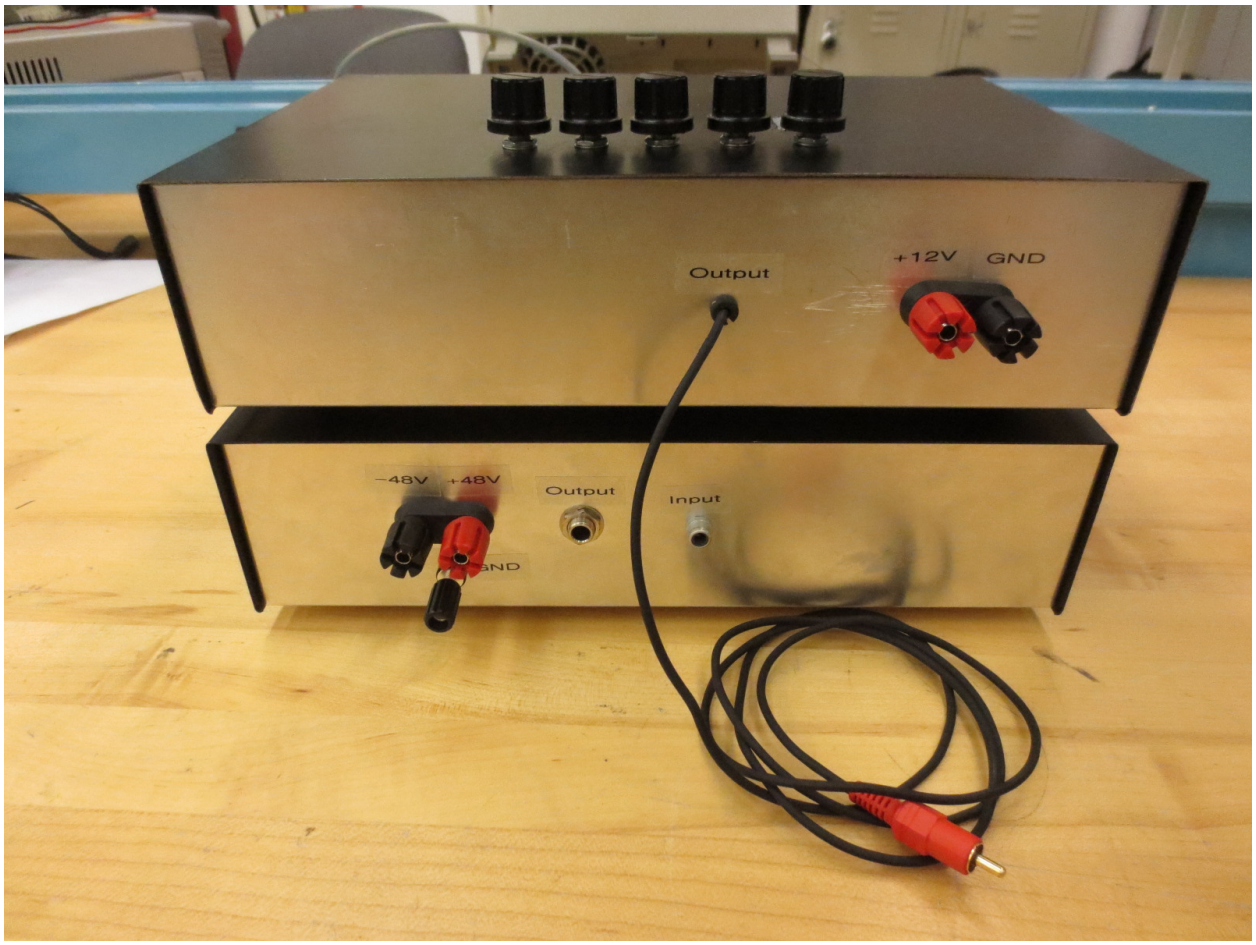
Appendix I: Operation Manual

Included Materials

Included are a high-voltage power supply, Equalizer, and Amplifier. A separate 12V power supply, not included, is required for Equalizer operation.

Setting Up

1. **DO NOT CONNECT THE POWER SUPPLIES TO THE WALL YET.**
2. Connect the +48V and -48V power supplies to the +48V and -48V connectors, respectively, on the Amplifier.
3. Connect the Ground on the 48V power supplies to the GND lug on the Amplifier.
4. Connect the 12V power supply +12V and GND to +12V and GND, respectively, on the Equalizer.
5. Connect the Equalizer output to the input of the Amplifier.
6. Connect a source (MP3 Player, computer, etc.) to the input of the Equalizer.
7. Connect a Speaker to the output jack on the back of the Amplifier.
8. Plug the high-voltage and 12V power supplies into the wall.



The Equalizer

The Equalizer can be used to adjust five frequency bands. Using the five knobs on top of the box, different emphasis can be given or taken away to parts of the audio, such as the treble or bass. Each knob also has a corresponding LED display to show the level of emphasis on that band.

A bypass switch is also provided. In the bypass position, the Equalizer settings will be ignored.

The Amplifier

The amplifier's volume level is set by the output volume of the source and cannot be adjusted on the amplifier itself. It should be adjusted at the source.

Appendix II: Early Alternative Versions

Amplifier

Our final design closely mirrors our initial block diagram, Fig. 1 (repeated below). However, we needed to completely change the implementations of certain blocks. Due to our high-efficiency requirement, we were very careful to avoid shoot-through current. Initially, we designed our own 555-based 300 kHz Sawtooth Oscillator (below). We planned to use this oscillator with a standalone comparator to produce the PWM signal. However, while researching methods to produce gate delay, we discovered the IRS2092 integrated circuit, which provides an all-in-one solution to many of our functional blocks. The IRS2092 provides an oscillator, comparator, and 2 variable delay gate drivers. Because ours is a full bridge design in which we use 4 MOSFETs, we require 2 IRS2092s, which became our final design.

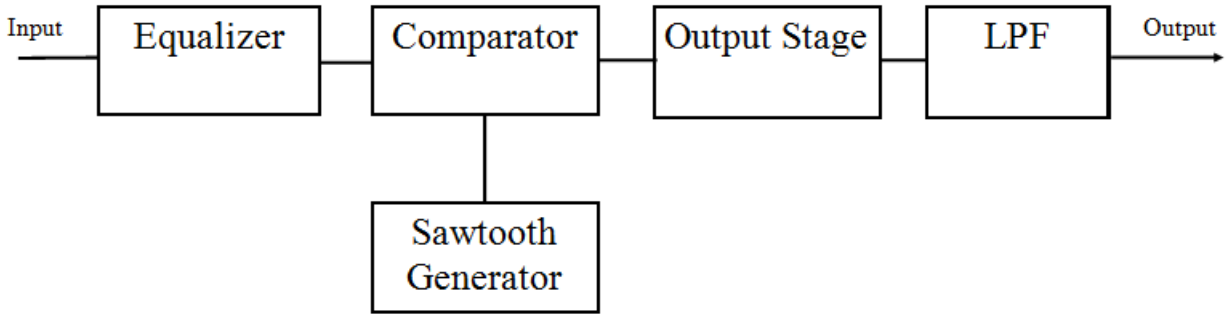
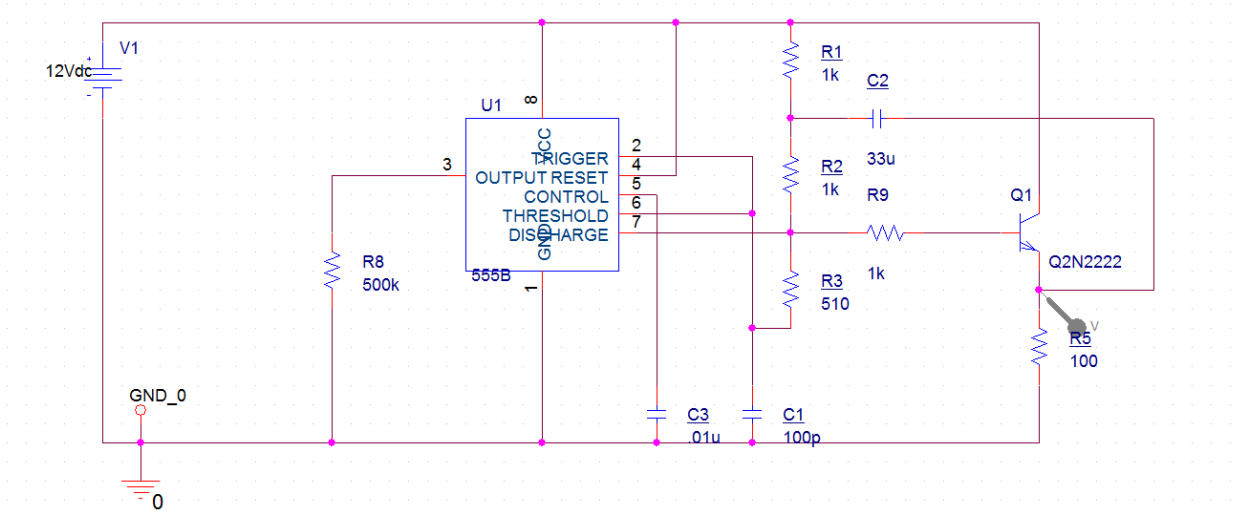
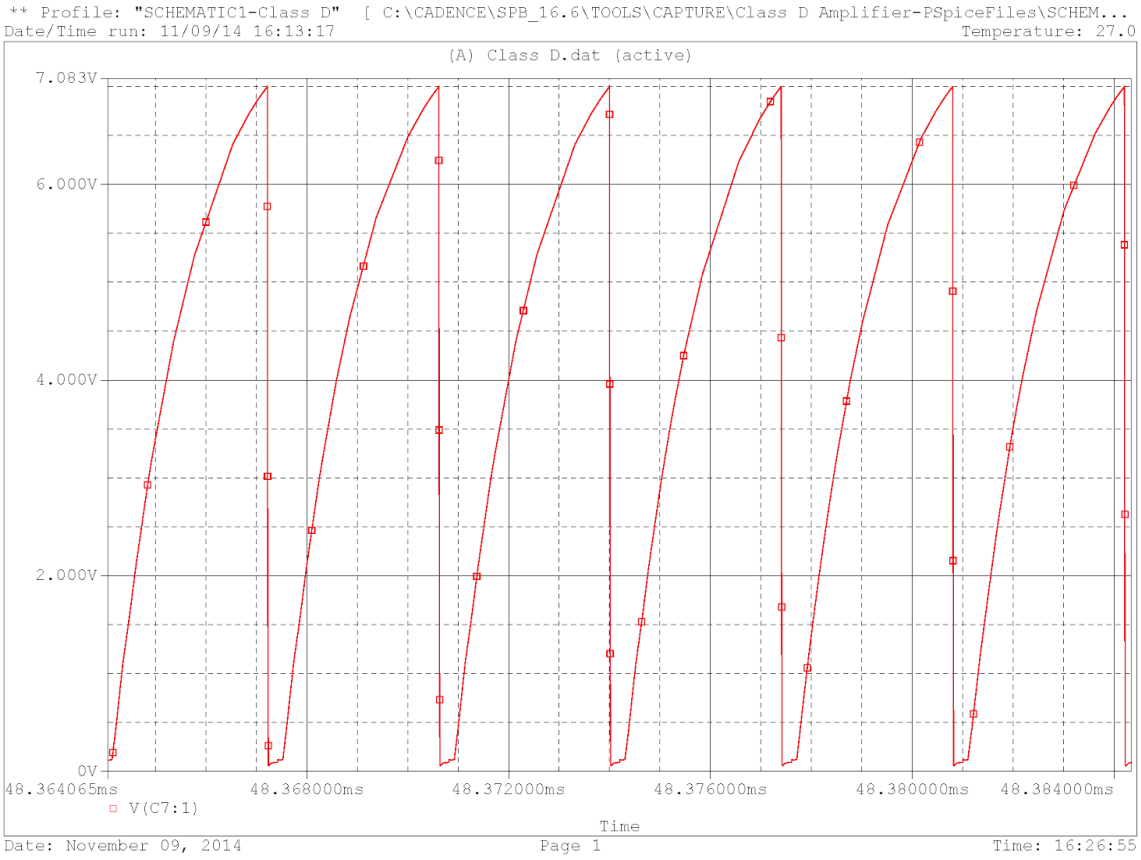


Figure 1. System block diagram

Our initial oscillator and its output is as follows:





This simulation output is not ideal, as the rising edge is significantly more curved than we would like. We found that the oscillator in the IRS2092 produces a much more ideal sawtooth output.

“It looks like a banana” - Dr. Gieger

Equalizer

The original project description specified a three-band Equalizer, but upon meeting with Prof. Fayed, we increased the requirement to five bands. Before drawing up our current Equalizer block diagram, we considered a series system. In this approach, five band-reject filters are put in series with gain in between each filter. We rejected this design because we believe it would not have resulted in the high SNR (96 dB) we require.

Appendix III: Other Considerations

In the course of this project, we encountered several challenges. Most of these were in the Amplifier section. We initially designed our own oscillator based on a 555 timer, which proved to be the wrong approach. As can be seen in Appendix II, the simulation output was not ideal. In retrospect, we should have worked towards an op-amp or discrete transistor based design, as this would have given us a much more ideal output.

However, after deciding on the IRS2092 approach, in which almost all functional blocks are included in the IC, we still encountered problems. After designing a PCB for this system and building the board up, we only found that it sparked instantaneously upon powering on. The lesson taken from this is that PCB design, especially on (relatively) high-power designs, is not a trivial task. Our traces were much too small and much too close together to support the kind of power we expected to be using.

In contrast, our Equalizer progress encountered few problems. We designed and simulated the entire system on the computer early first semester, and after finalizing the design in simulation, found that it worked just as expected on a breadboard early second semester. We then spent a couple weeks working on the PCB design. Due to our methodical approach, we found that the PCB implementation worked just as expected, and we still had time left to implement an Arduino-based user feedback system.

Although we had split up the team into EQ and Amplifier sub-teams, we would have been better off focusing on the Amplifier portion much earlier, as that proved to be a much more involved task. Had we done that, we could have made all of our mistakes and then corrected them to yield a fully working product. Instead, we have a working EQ and a burnt-up Amplifier board.

Appendix IV: Code

This is the code that controls the EQ display LEDs.

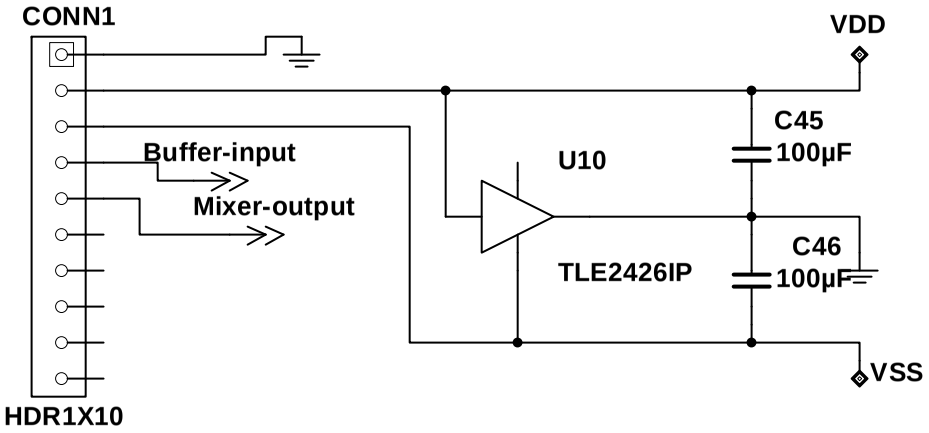
```
const int analogPin = A0;   // the pin that the 1st potentiometer is attached to
const int ledCount = 10;    // the number of LEDs in the 1st bar graph

const int analogPin_2 = A1 ; // the pin that the 2nd potentiometer is attached to
const int ledCount_2 = 10; // the number of LEDs in the 2nd bar graph

const int analogPin_3 = A5 ; // the pin that the 3rd potentiometer is attached to
const int ledCount_3 = 10; // the number of LEDs in the 3rd bar graph

const int analogPin_4 = A3 ; // the pin that the 4th potentiometer is attached to
const int ledCount_4 = 10; // the number of LEDs in the 4th bar graph

const int analogPin_5 = A4 ; // the pin that the 5th potentiometer is attached to
const int ledCount_5 = 10; // the number of LEDs in the 5th bar graph

int ledPins[] = {
  4, 5, 6, 7,8,9,10,11,12,13 };   // an array of pin numbers to which the 1st bar graph is attached

int ledPins_2[] = {
  19,18,17,16,15,14,0,1,2,3 };   // an array of pin6, numbers to which the 2nd bar graph attached

int ledPins_3[] = {
36,34,32,30,28,26,24,22,21,20 };   // an array of pin numbers to which the 3rd bar graph attached

int ledPins_4[] = {
53,51,52,50,48,46,44,42,40,38 };   // an array of pin numbers to which the 4th bar graph is attached

int ledPins_5[] = {
49,47,45,43,41,39,37,35,33,31 };   // an array of pin numbers to which the 5th bar graph is attached

void setup() {
  // loop over the pin array and set them all to output:
  pinMode(A0,INPUT);
  pinMode(A1,INPUT);
  pinMode(A2,INPUT);
  pinMode(A3,INPUT);
  pinMode(A4,INPUT);

// set each array to output mode
```

```
  for (int thisLed = 0; thisLed < ledCount; thisLed++) {
   pinMode(ledPins[thisLed], OUTPUT);
  }

   for (int thisLed_2 = 0; thisLed_2 < ledCount_2; thisLed_2++) {
   pinMode(ledPins_2[thisLed_2], OUTPUT);
  }

   for (int thisLed_3 = 0; thisLed_3 < ledCount_3; thisLed_3++) {
   pinMode(ledPins_3[thisLed_3], OUTPUT);
  }

   for (int thisLed_4 = 0; thisLed_4 < ledCount_4; thisLed_4++) {
   pinMode(ledPins_4[thisLed_4], OUTPUT);
  }

   for (int thisLed_5 = 0; thisLed_5 < ledCount_5; thisLed_5++) {
   pinMode(ledPins_5[thisLed_5], OUTPUT);
  }


}


void loop(){


  int sensorReading = analogRead(analogPin);  // reading the relative potentiometer voltage
  int ledLevel = map(sensorReading, 0, 1023, 9, 0); //maping the reading to 10 levels

  int sensorReading_2 = analogRead(analogPin_2);
  int ledLevel_2 = map(sensorReading_2, 0, 1023, 9, 0);

  int sensorReading_3 = analogRead(analogPin_3);
  int ledLevel_3 = map(sensorReading_3, 0, 1023, 9, 0);

  int sensorReading_4 = analogRead(analogPin_4);
  int ledLevel_4 = map(sensorReading_4, 0, 1023, 9, 0);

  int sensorReading_5 = analogRead(analogPin_5);
  int ledLevel_5 = map(sensorReading_5, 0, 1023, 9, 0);

 digitalWrite(ledPins[ledLevel], HIGH);  // lighting up the level that the potentiometers are at
```

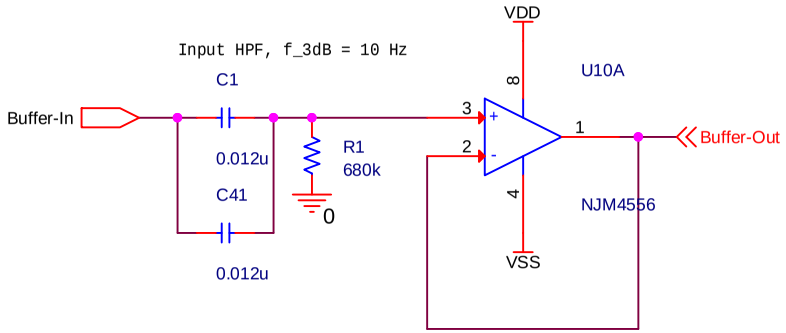
```
 for (int thisLed = 0; thisLed < ledCount; thisLed++) {   //shuting down the other levels
    if (thisLed != ledLevel) {
      digitalWrite(ledPins[thisLed], LOW);
    }
 }

 digitalWrite(ledPins_2[ledLevel_2], HIGH);
 for (int thisLed_2 = 0; thisLed_2 < ledCount_2; thisLed_2++) {
    if (thisLed_2 != ledLevel_2) {
      digitalWrite(ledPins_2[thisLed_2], LOW);
    }
}

 digitalWrite(ledPins_3[ledLevel_3], HIGH);
 for (int thisLed_3 = 0; thisLed_3 < ledCount_3; thisLed_3++) {
    if (thisLed_3 != ledLevel_3) {
      digitalWrite(ledPins_3[thisLed_3], LOW);
    }
}

 digitalWrite(ledPins_4[ledLevel_4], HIGH);
 for (int thisLed_4 = 0; thisLed_4 < ledCount_4; thisLed_4++) {
    if (thisLed_4 != ledLevel_4) {
      digitalWrite(ledPins_4[thisLed_4], LOW);
    }
}

 digitalWrite(ledPins_5[ledLevel_5], HIGH);
 for (int thisLed_5 = 0; thisLed_5 < ledCount_5; thisLed_5++) {
    if (thisLed_5 != ledLevel_5) {
      digitalWrite(ledPins_5[thisLed_5], LOW);
    }
}

}
```

Appendix V: Equalizer Schematics

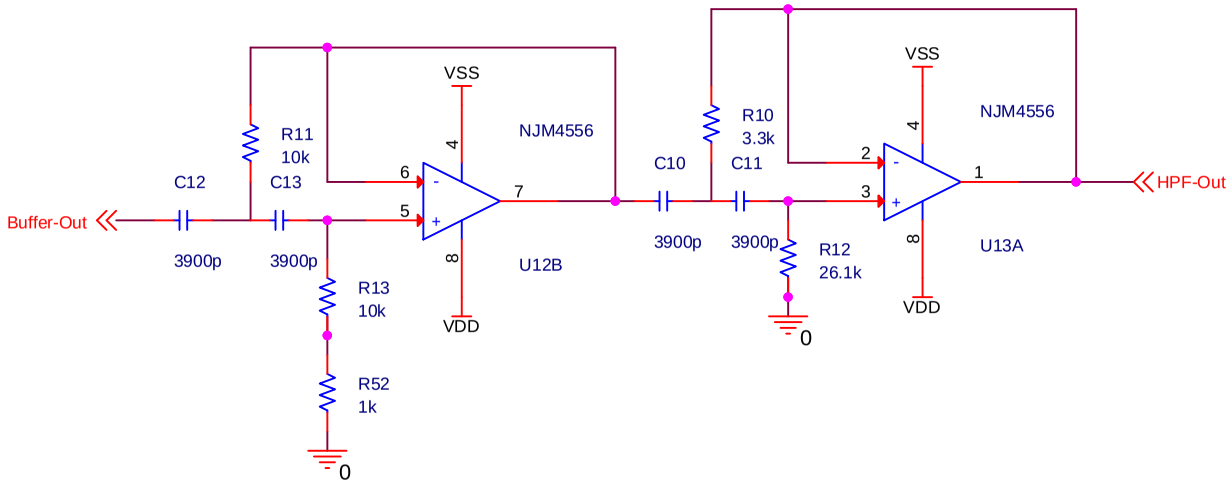
In the following pages are our Schematics for all functional blocks of the Equalizer not included earlier in this document.



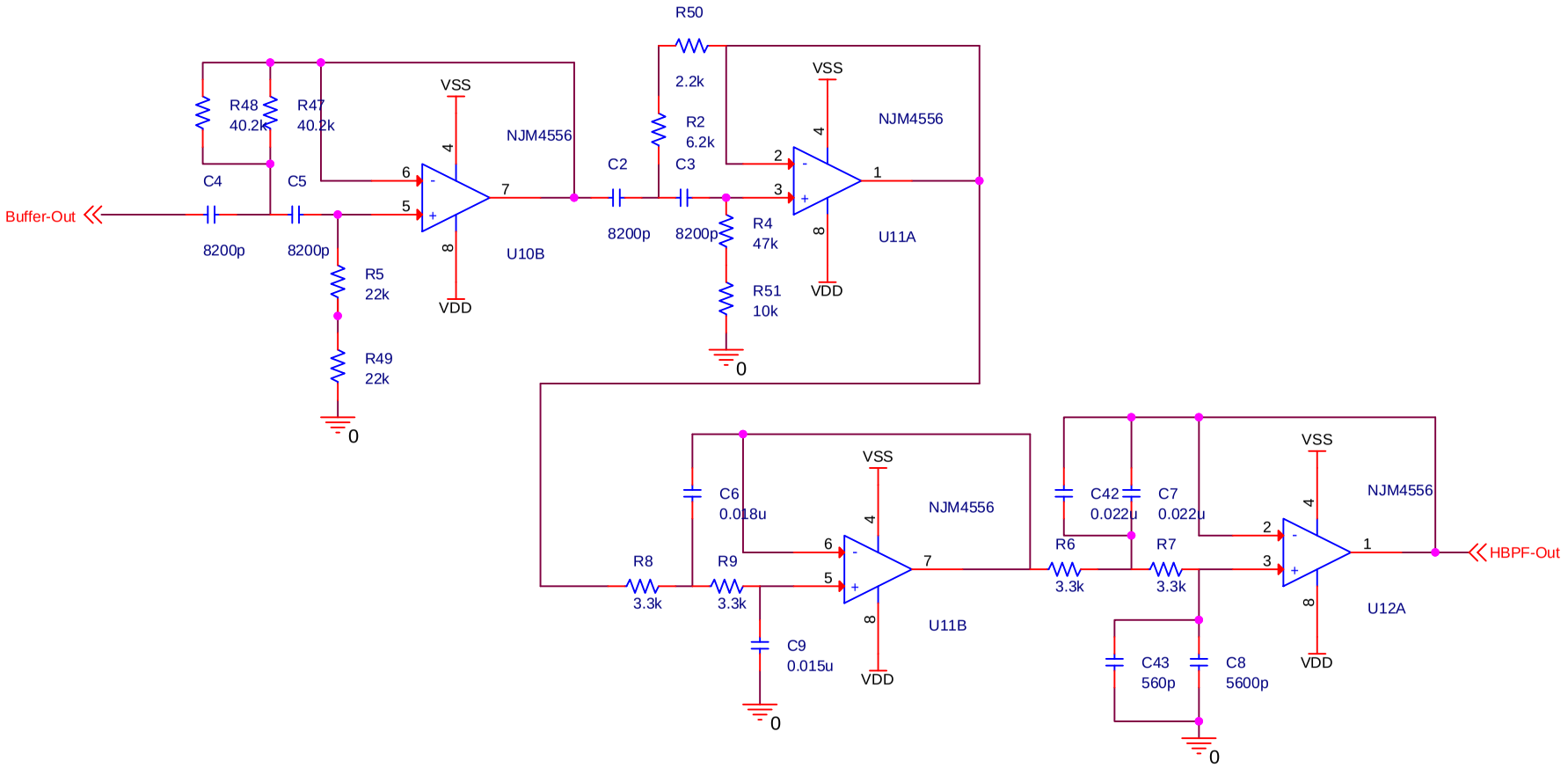
Title: Virtual Ground	Desc.: Produces a 6V virtual ground for Equalizer	
Designed by:	Document No:	Revision: 3
Checked by:	Date: 4/28/2015	Size: A
Approved by:	Sheet 2 of 8	



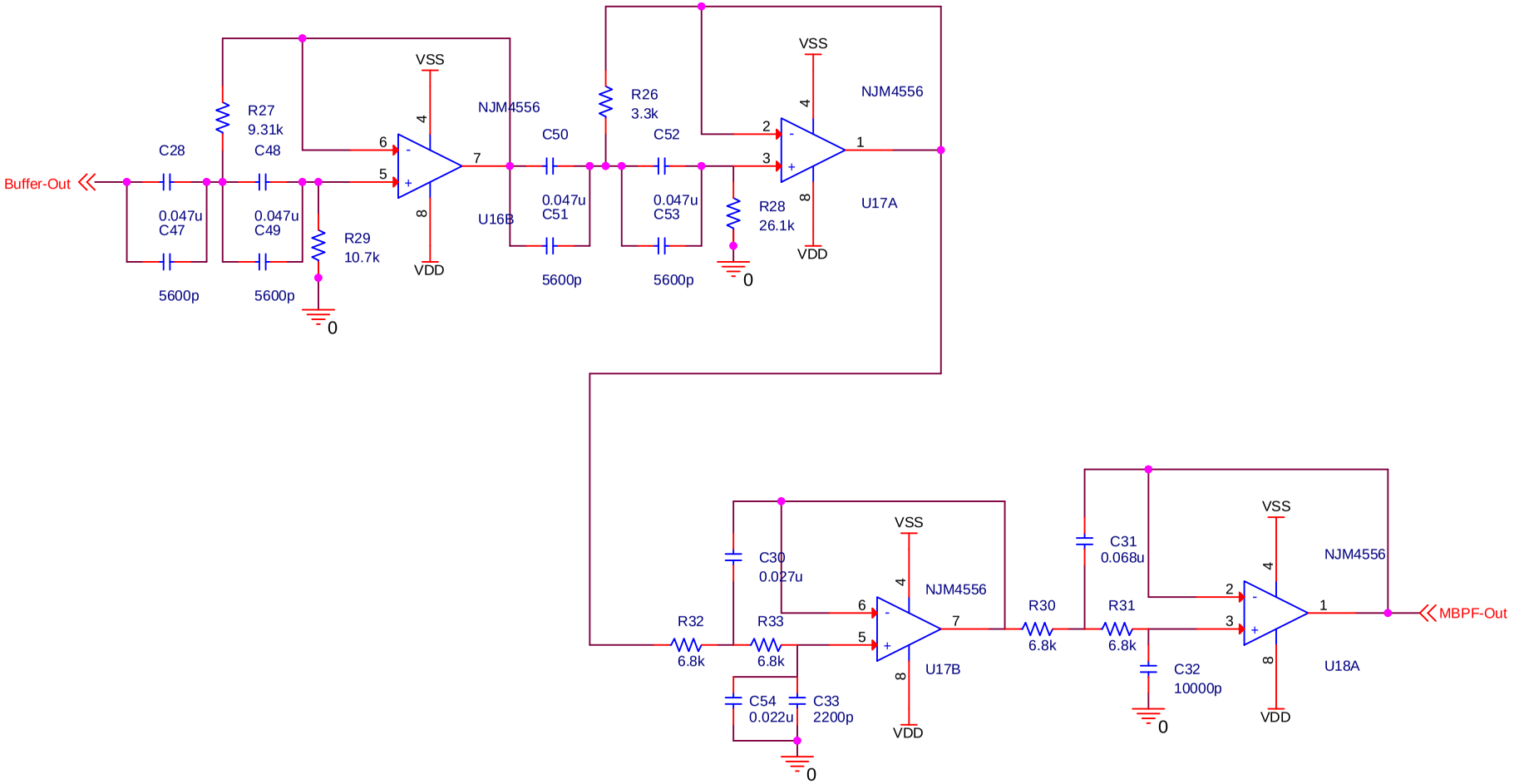
Title: Input Buffer		
Size: Custom	Document Number: 1	Rev: 3
Date: Sunday, October 19, 2014	Sheet 1 of 8	



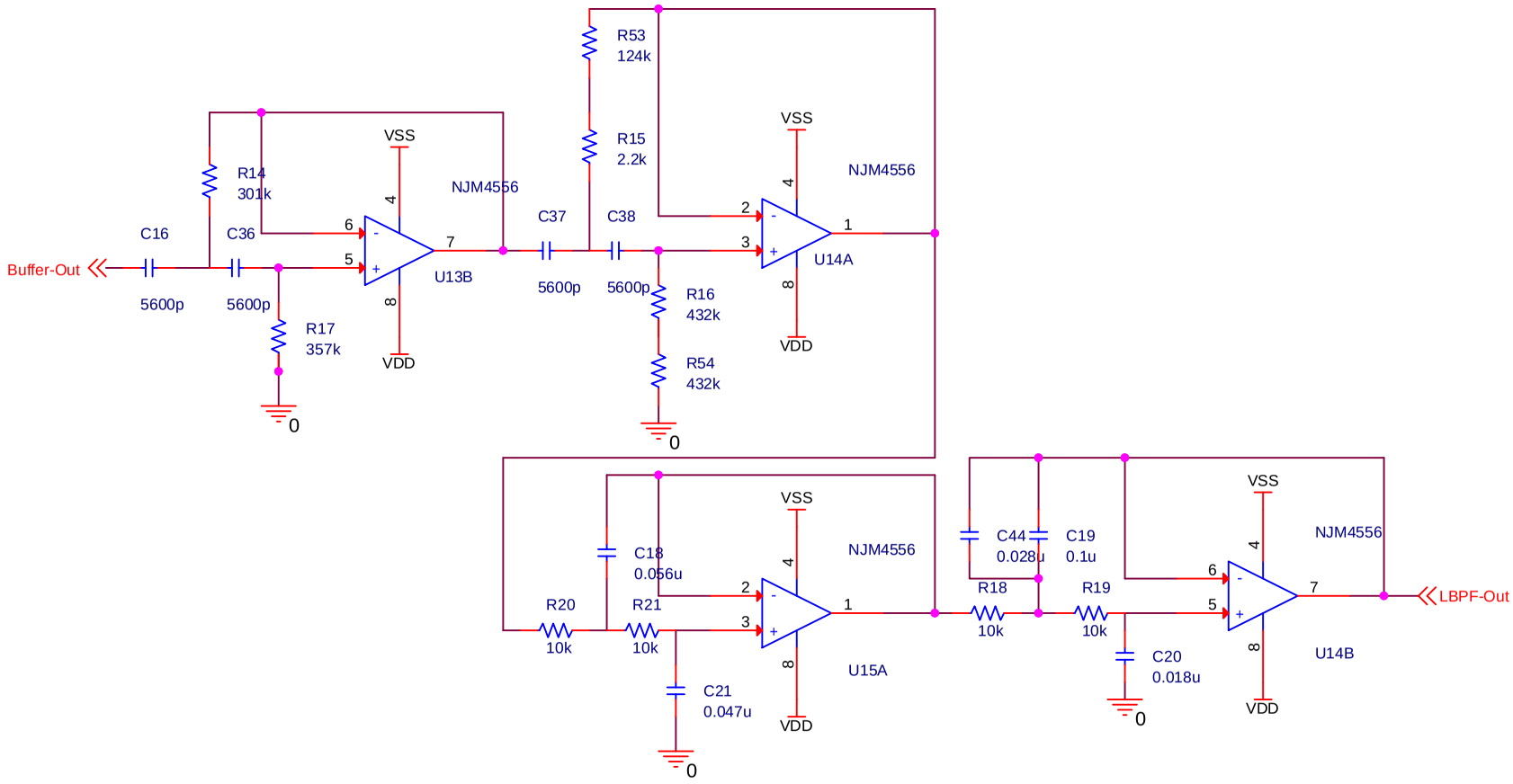
Title	High Pass Filter, 4 kHz	
Size: Custom3	Document Number	Rev: 4
Date: Sunday, October 26, 2014	Sheet 3 of 8	



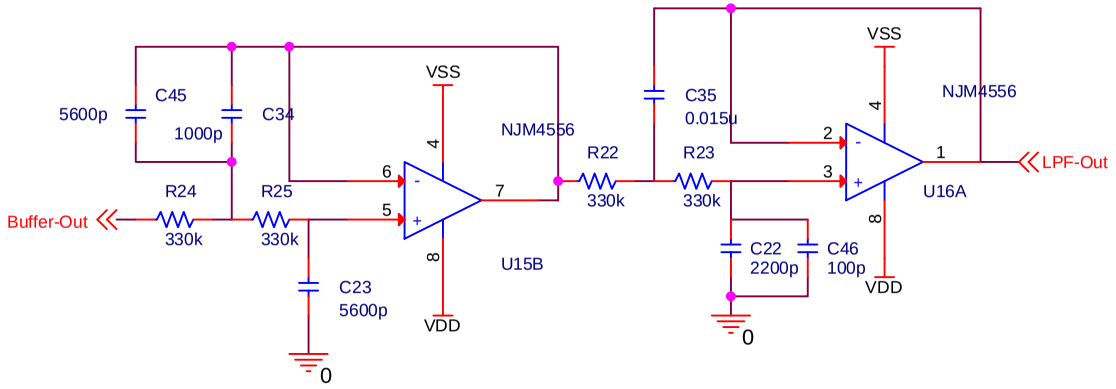
Title	High Band Pass Filter, 900 Hz - 3 kHz	
Size: Custom2	Document Number	Rev: 4
Date: Sunday, October 26, 2014	Sheet 2 of 8	



Title	Mid Band Pass Filter, 300 Hz - 900 Hz	
Size: Custom6	Document Number	Rev: 4
Date: Sunday, October 26, 2014	Sheet 6 of 8	



Title	Low Band Pass Filter, 90 Hz - 325 Hz	
Size: Custom4	Document Number	Rev: 4
Date: Sunday, October 26, 2014	Sheet 4 of 8	



Title	Low Pass Filter, 80 Hz	
Size: Custom5	Document Number	Rev: 4
Date: Sunday, October 26, 2014	Sheet 5 of 8	